OIPE JC71
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PATENT & TRADEMARK OFFICE

FIG. 1

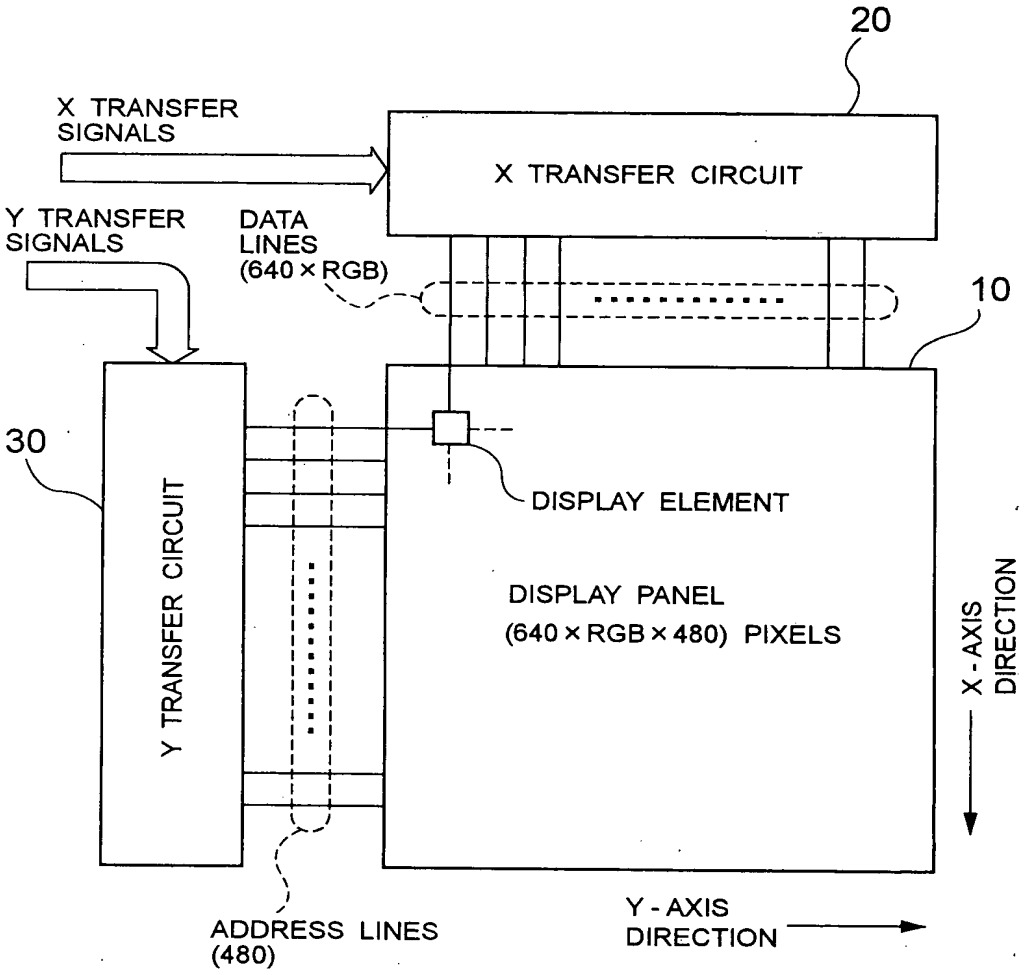


FIG. 2

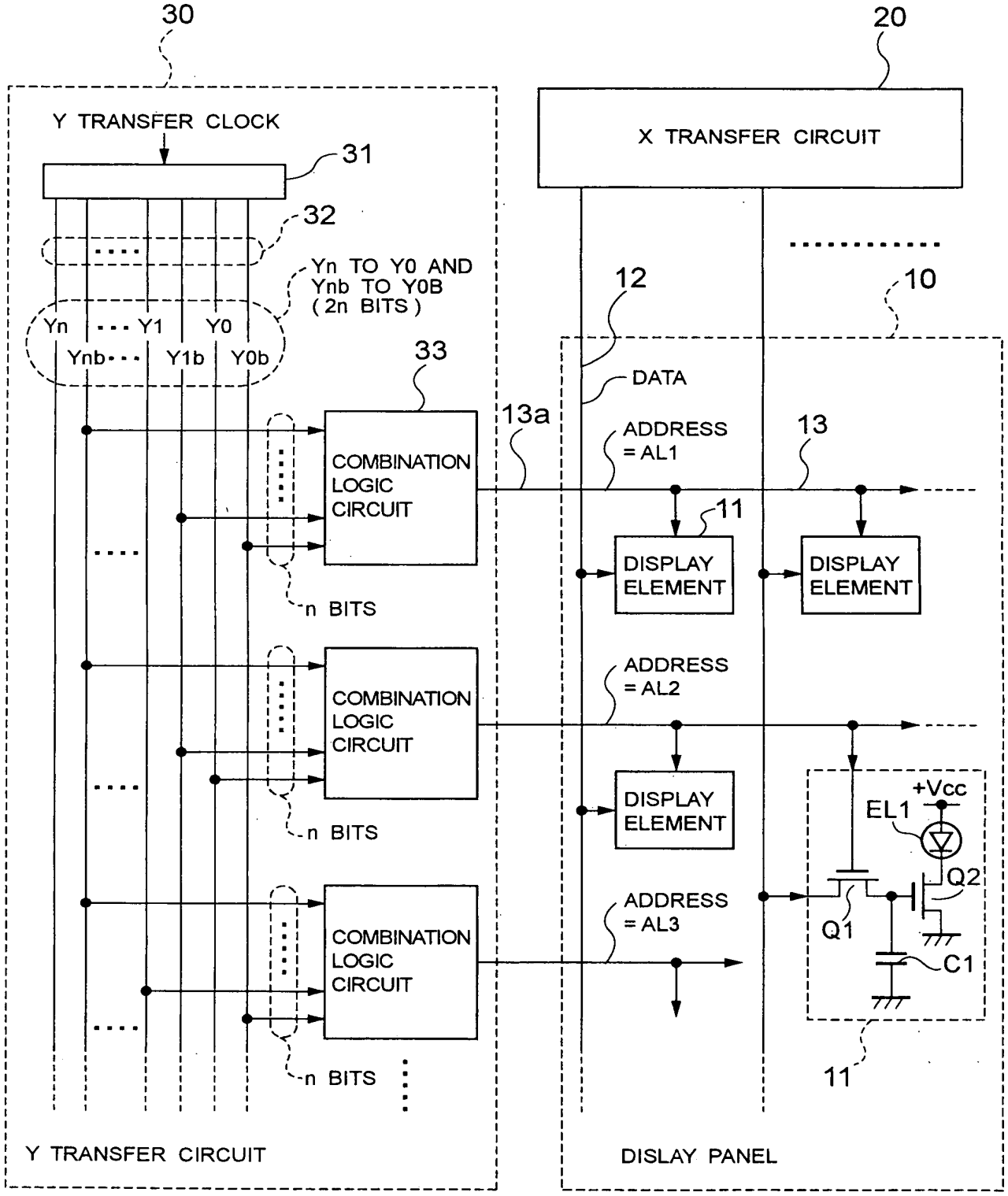

30
20
Y TRANSFER CLOCK
31
X TRANSFER CIRCUIT
32
Yn TO Y0 AND
Ynb TO Y0B
(2n BITS)
Yn
Y1
Y0
Ynb
Y1b
Y0b
12
10
33
DATA
13a
ADDRESS
= AL1
13
COMBINATION
LOGIC
CIRCUIT
11
DISPLAY
ELEMENT
DISPLAY
ELEMENT
n BITS
ADDRESS
= AL2
COMBINATION
LOGIC
CIRCUIT
DISPLAY
ELEMENT
+Vcc
EL1
Q2
Q1
C1
n BITS
ADDRESS
= AL3
COMBINATION
LOGIC
CIRCUIT
n BITS
11
Y TRANSFER CIRCUIT
DISLAY PANEL

FIG. 3

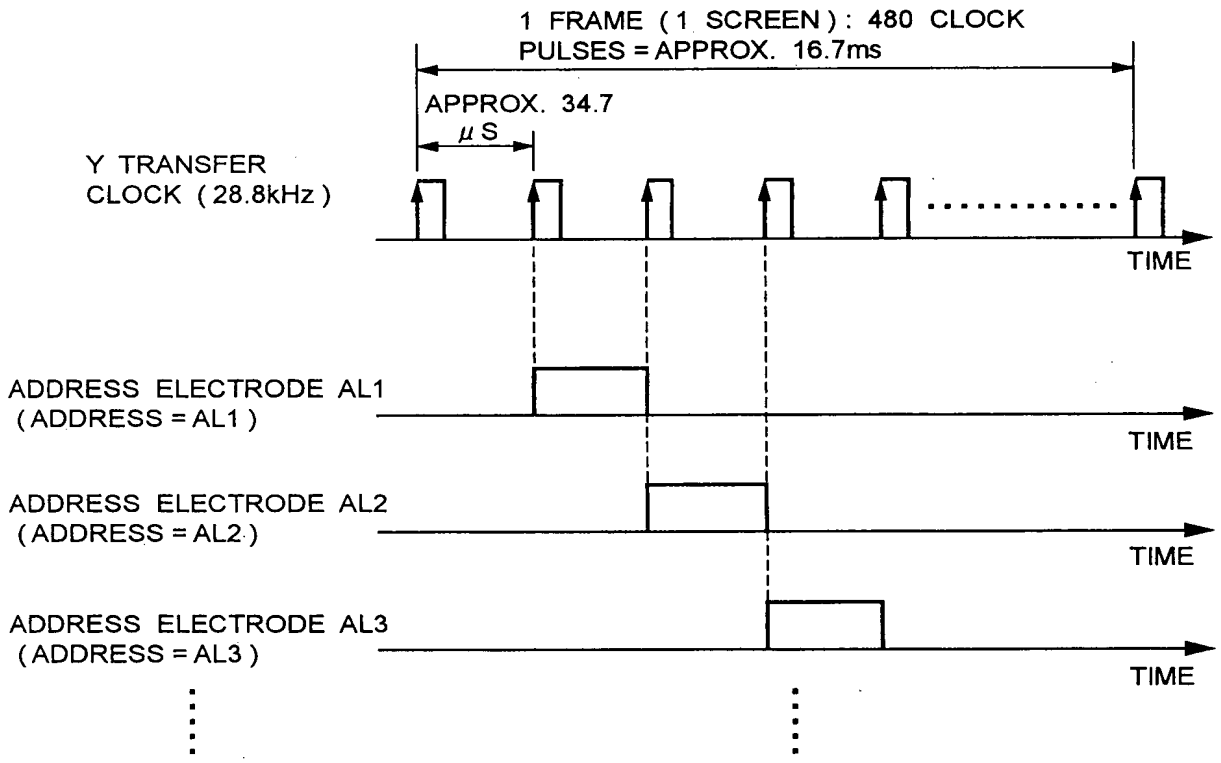

1 FRAME (1 SCREEN) : 480 CLOCK
PULSES = APPROX. 16.7ms
APPROX. 34.7
μ S
Y TRANSFER
CLOCK (28.8kHz)
TIME
ADDRESS ELECTRODE AL1
(ADDRESS = AL1)
TIME
ADDRESS ELECTRODE AL2
(ADDRESS = AL2)
TIME
ADDRESS ELECTRODE AL3
(ADDRESS = AL3)
TIME

FIG. 4

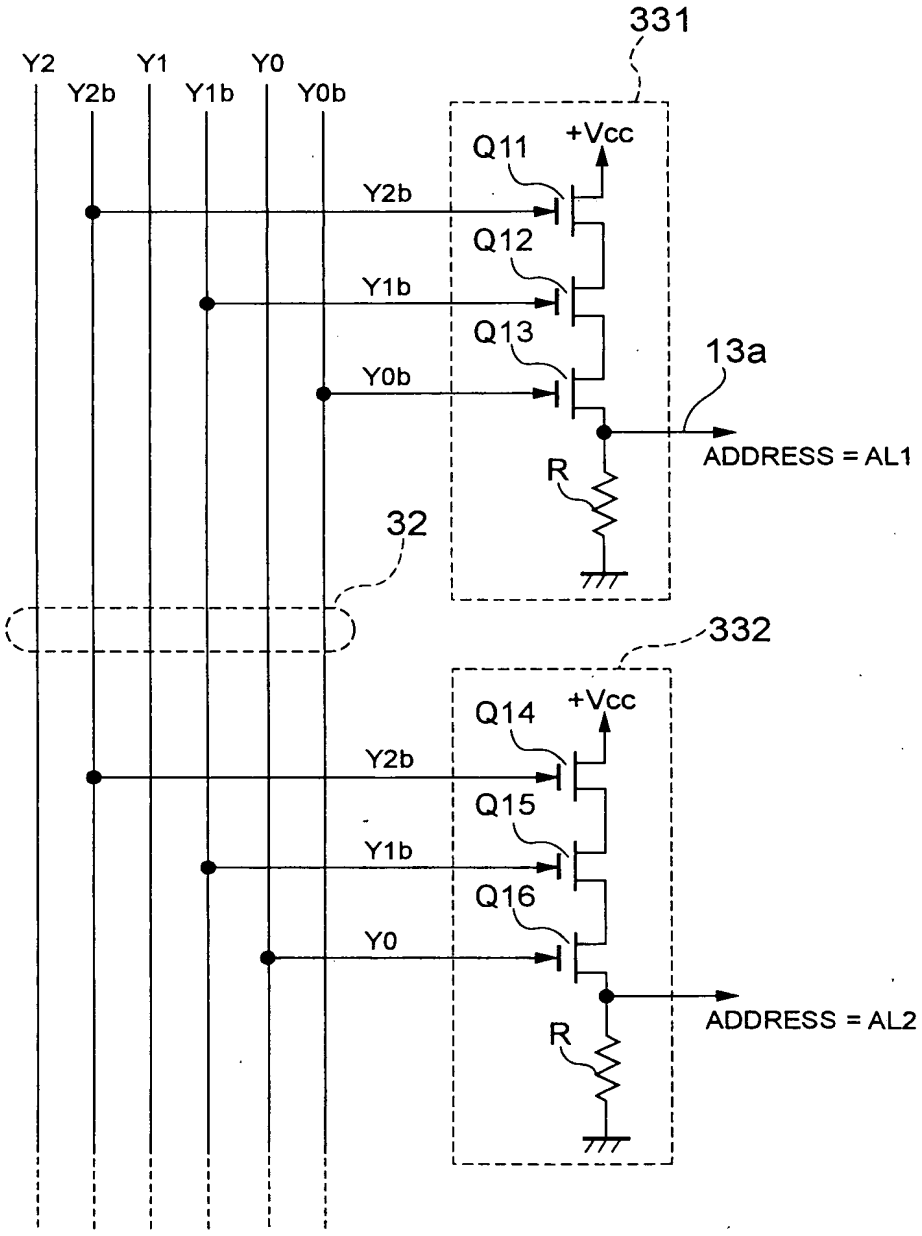

331
Y2
Y2b
Y1
Y1b
Y0
Y0b
Q11
+Vcc
Y2b
Q12
Y1b
Q13
13a
Y0b
ADDRESS = AL1
R
32
332
Q14
+Vcc
Y2b
Q15
Y1b
Q16
Y0
ADDRESS = AL2
R

FIG. 5

ADDRESS AL	RELATION BETWEEN CODE GROUP SUPERPOSED ON DATA CONTROL LINE GROUP (Y2 TO Y0 AND Y2b TO Y0b) AND DECODED ADDRESS					
	BINARY CODE			INVERTED BINARY CODE		
	Y2	Y1	Y0	Y2b	Y1b	Y0b
AL=1	0	0	0	1	1	1
AL=2	0	0	1	1	1	0
AL=3	0	1	0	1	0	1
AL=4	0	1	1	1	0	0
AL=5	1	0	0	0	1	1
AL=6	1	0	1	0	1	0
AL=7	1	1	0	0	0	1
AL=8	1	1	1	0	0	0

FIG. 6

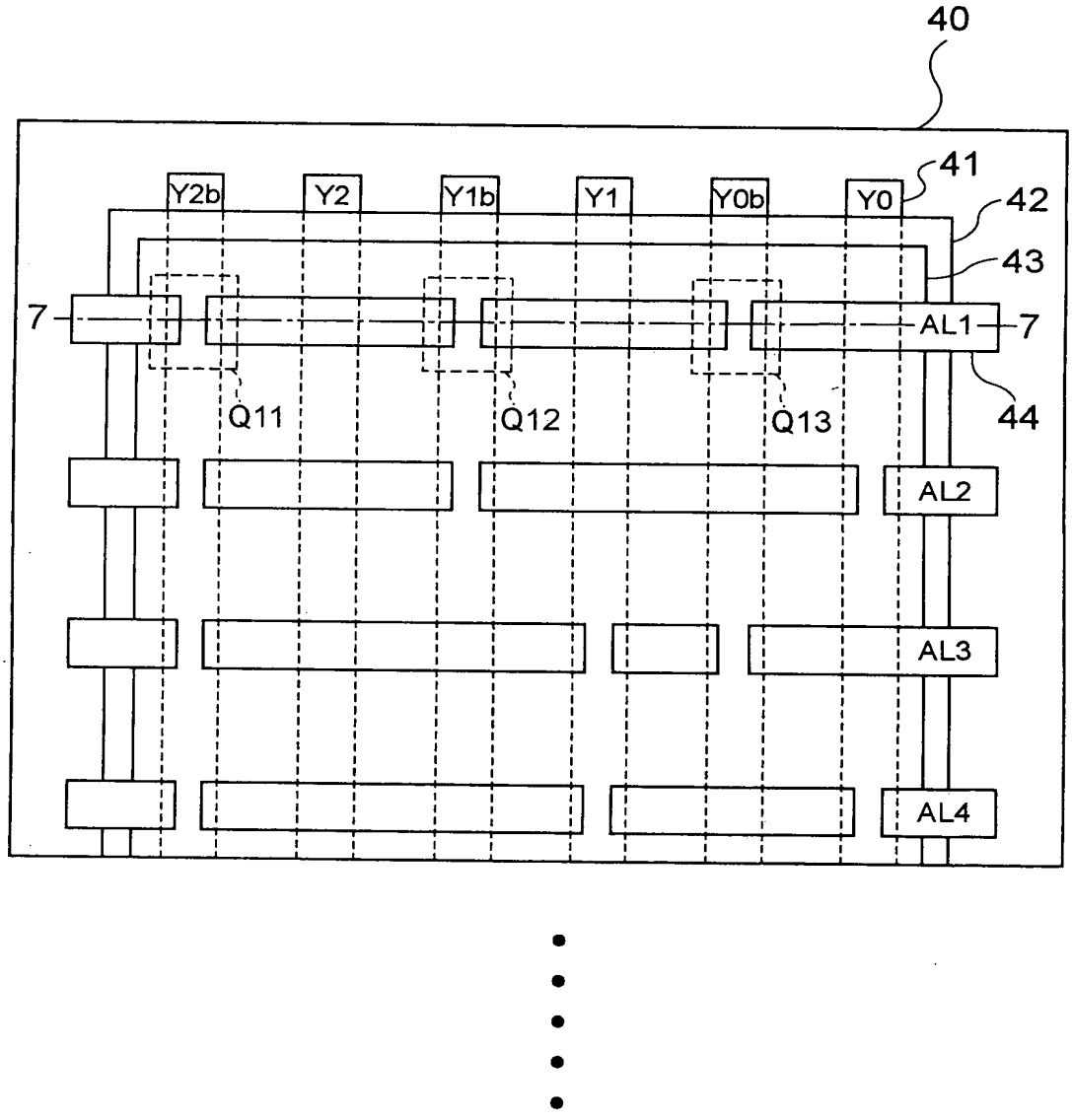


FIG. 7

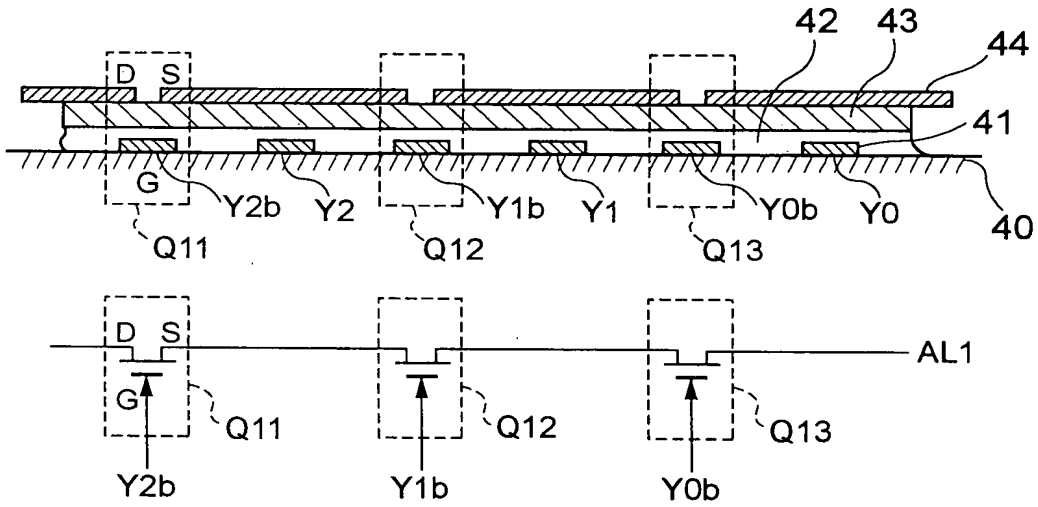

42
43
44
41
D
S
G
Y2b
Y2
Y1b
Y1
Y0b
Y0
40
Q11
Q12
Q13
D
S
AL1
G
Q11
Q12
Q13
Y2b
Y1b
Y0b

FIG. 8

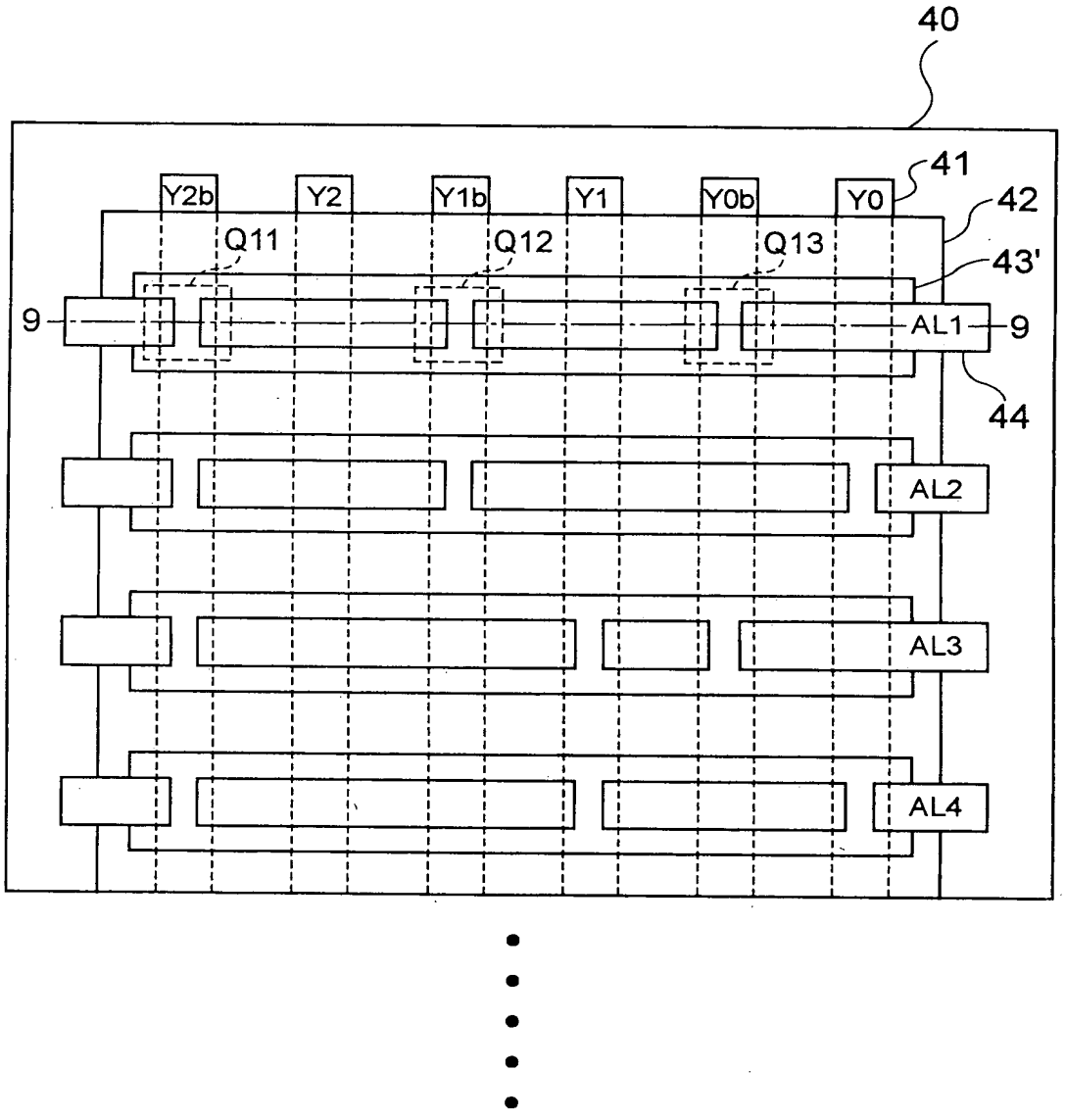


FIG. 9

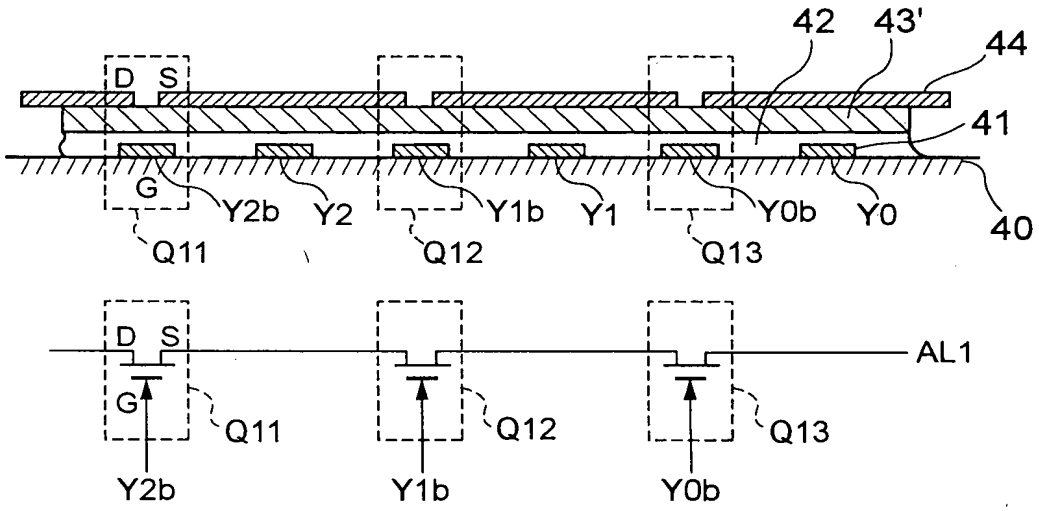


FIG. 10

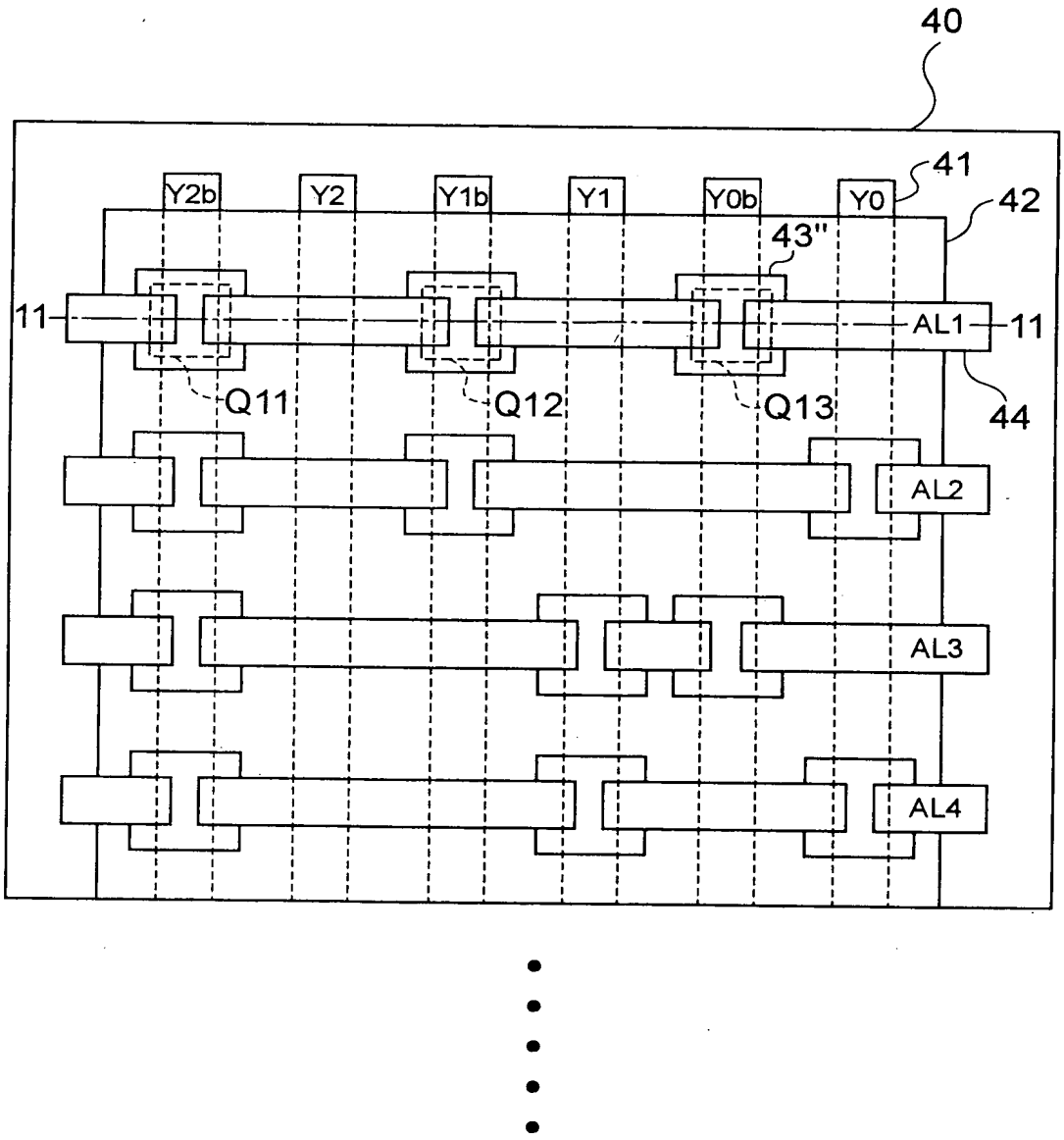

40
41
42
Y2b
Y2
Y1b
Y1
Y0b
Y0
43"
11
AL1
11
Q11
Q12
Q13
44
AL2
AL3
AL4

FIG. 11

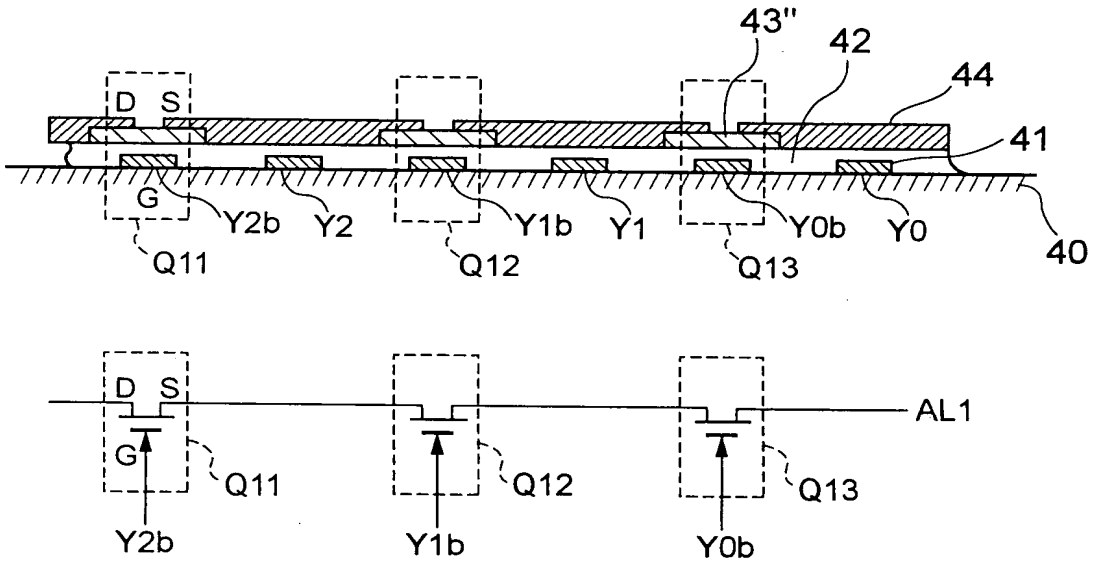


FIG. 12

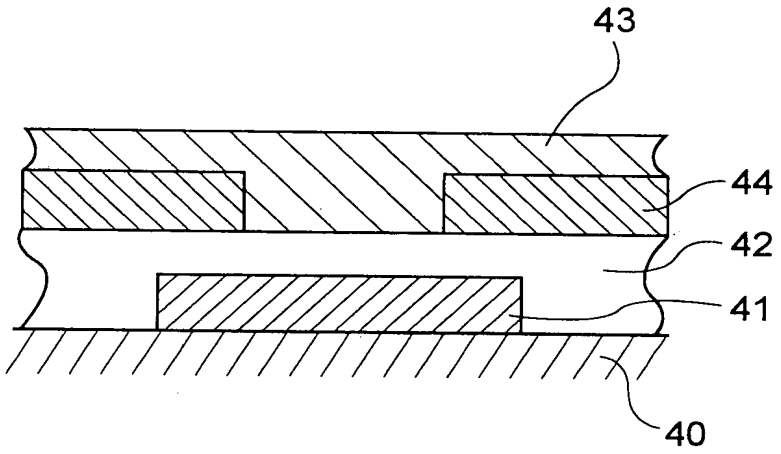


FIG. 13

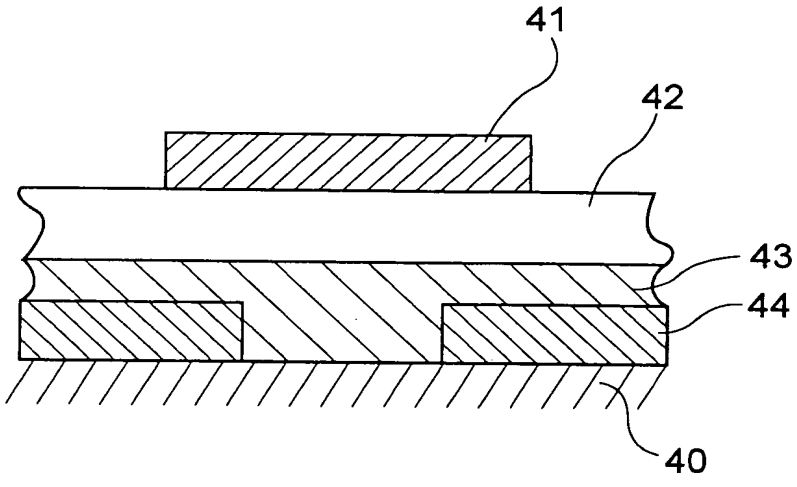


FIG. 14

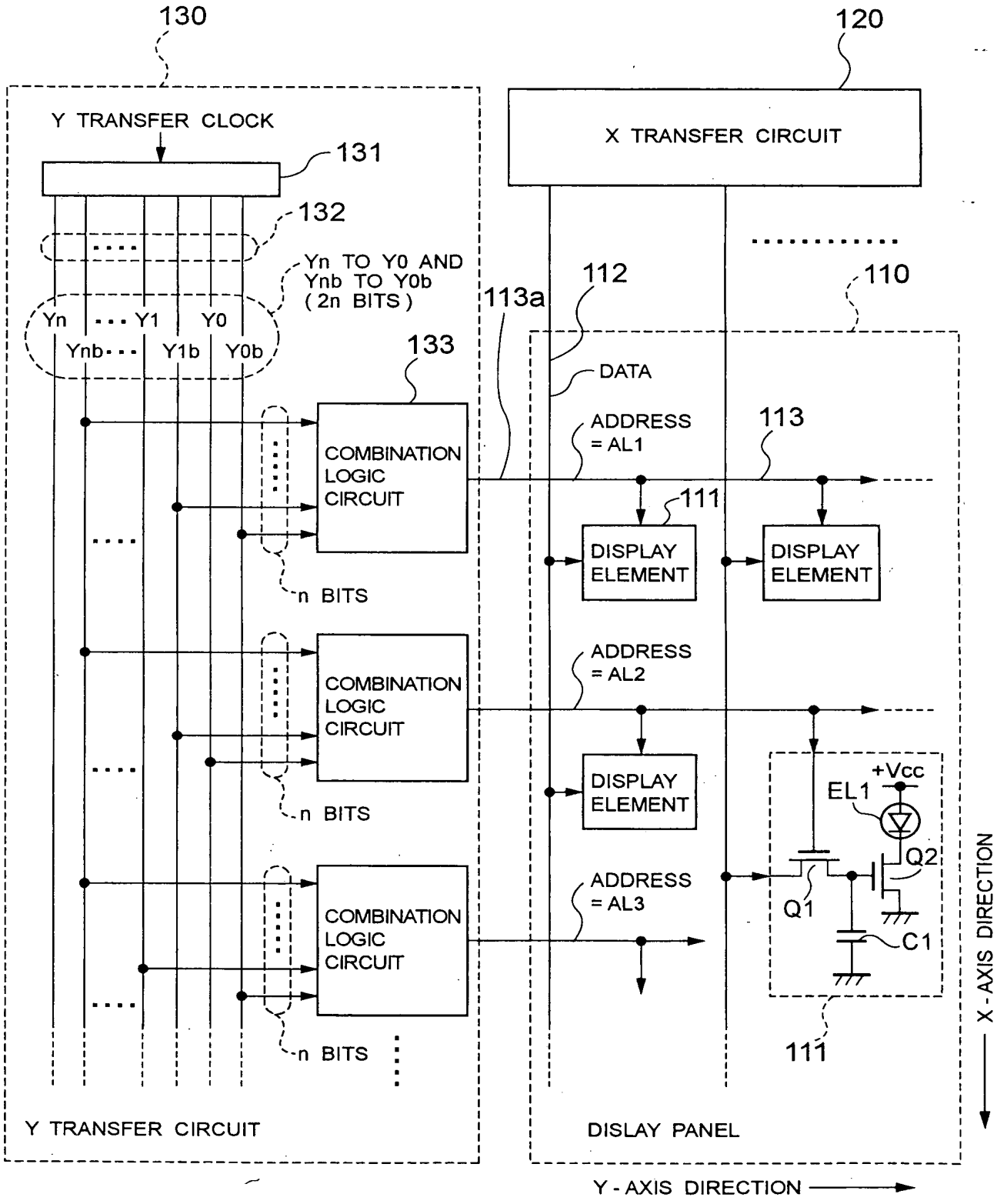

130
120
Y TRANSFER CLOCK
131
X TRANSFER CIRCUIT
132
Yn TO Y0 AND
Ynb TO Y0b
(2n BITS)
Yn ... Y1 Y0
Ynb ... Y1b Y0b
133
112
110
113a
DATA
ADDRESS
= AL1
113
111
COMBINATION
LOGIC
CIRCUIT
DISPLAY
ELEMENT
n BITS
ADDRESS
= AL2
ADDRESS
= AL3
+Vcc
EL1
Q2
Q1
C1
X - AXIS DIRECTION
Y TRANSFER CIRCUIT
DISLAY PANEL
Y - AXIS DIRECTION

FIG. 15

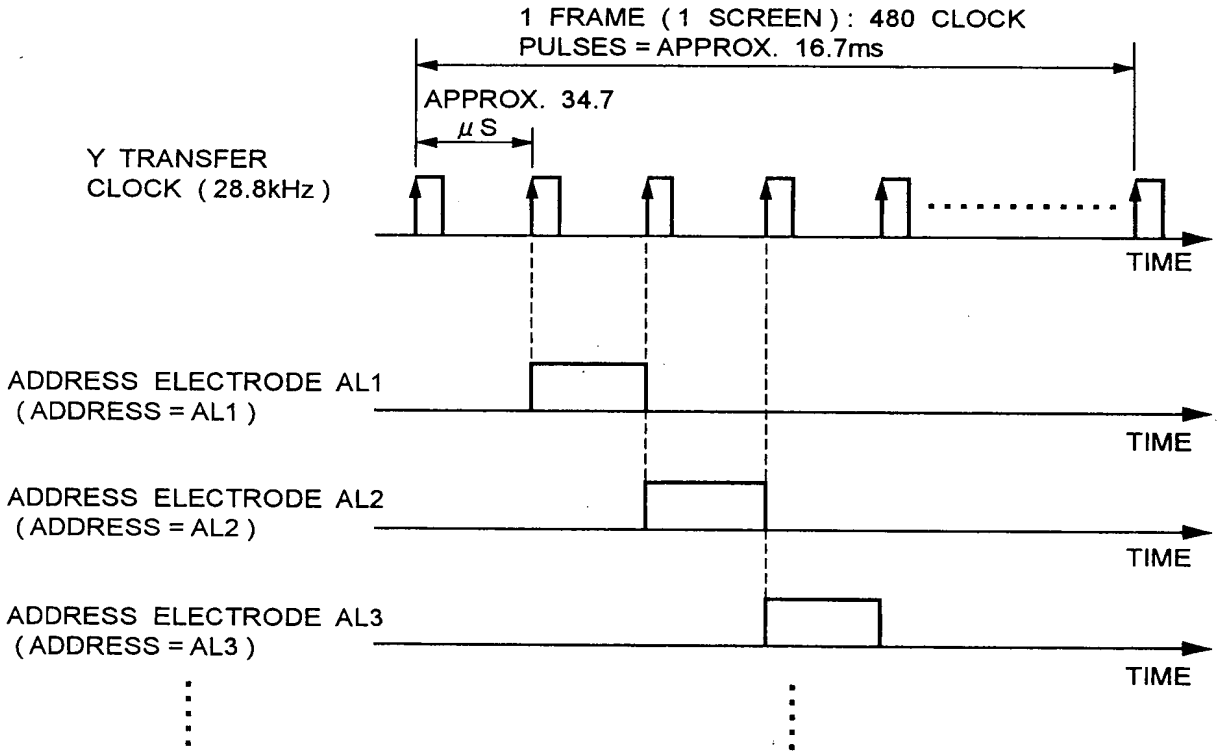

1 FRAME (1 SCREEN) : 480 CLOCK
PULSES = APPROX. 16.7ms
APPROX. 34.7
μS
Y TRANSFER
CLOCK (28.8kHz)
TIME
ADDRESS ELECTRODE AL1
(ADDRESS = AL1)
TIME
ADDRESS ELECTRODE AL2
(ADDRESS = AL2)
TIME
ADDRESS ELECTRODE AL3
(ADDRESS = AL3)
TIME

FIG. 16

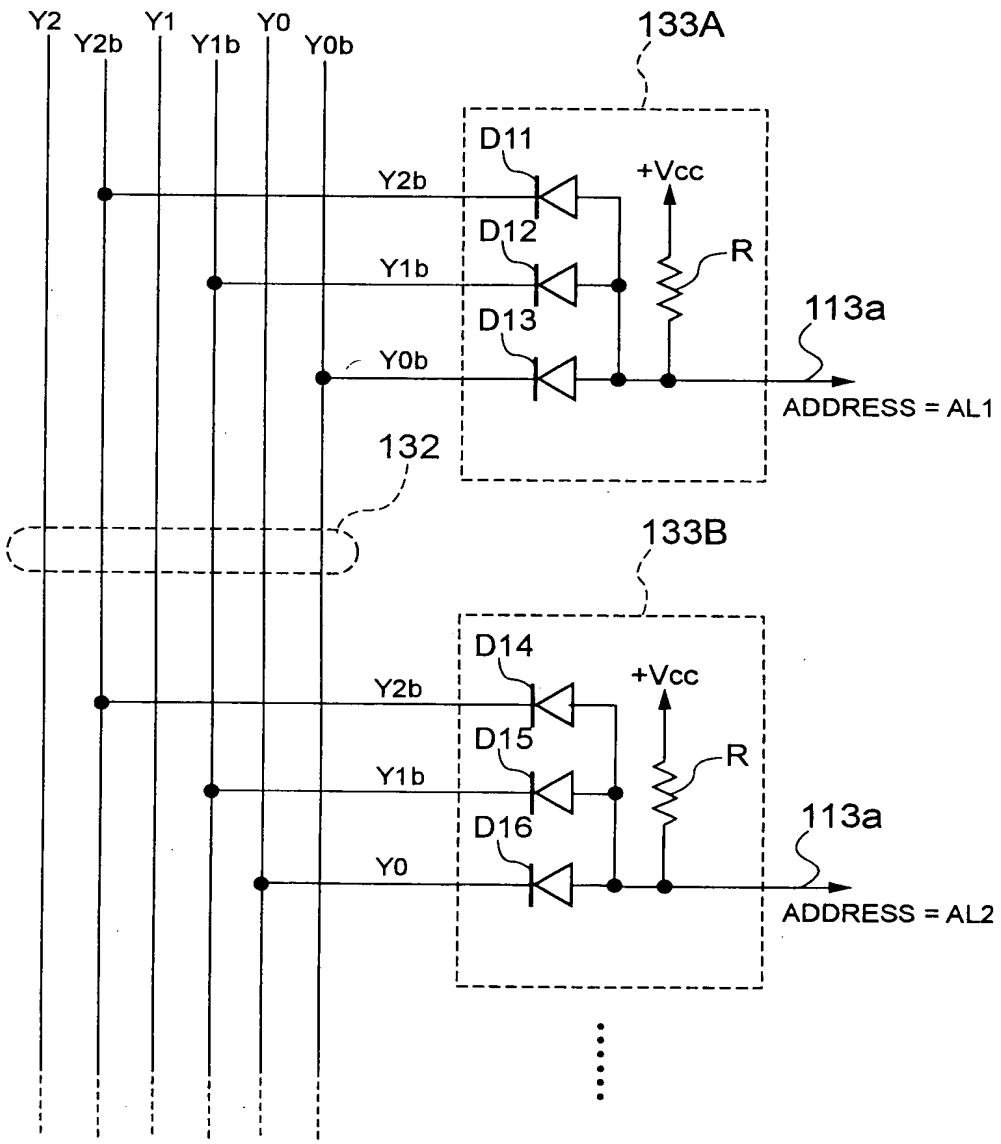

Y2
Y2b
Y1
Y1b
Y0
Y0b
133A
D11
+Vcc
Y2b
D12
R
Y1b
D13
113a
Y0b
ADDRESS = AL1
132
133B
D14
+Vcc
Y2b
D15
R
Y1b
D16
113a
Y0
ADDRESS = AL2

FIG. 17

ADDRESS AL	RELATION BETWEEN CODE GROUP SUPERPOSED ON DATA CONTROL LINE GROUP (Y2 TO Y0 AND Y2b TO Y0b) AND DECODED ADDRESS					
	BINARY CODE			INVERTED BINARY CODE		
	Y2	Y1	Y0	Y2b	Y1b	Y0b
AL=1	0	0	0	1	1	1
AL=2	0	0	1	1	1	0
AL=3	0	1	0	1	0	1
AL=4	0	1	1	1	0	0
AL=5	1	0	0	0	1	1
AL=6	1	0	1	0	1	0
AL=7	1	1	0	0	0	1
AL=8	1	1	1	0	0	0

FIG. 18

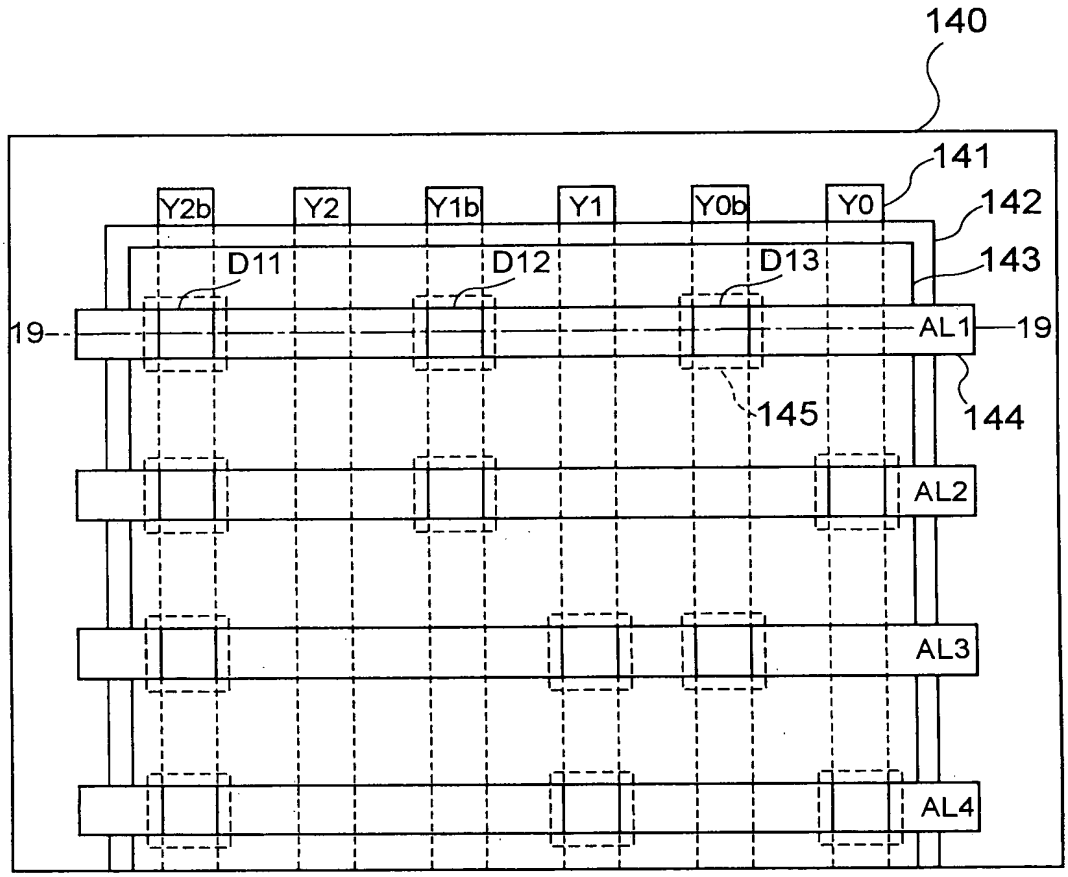

140
141
142
143
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
19
AL1
19
145
144
AL2
AL3
AL4

FIG. 19

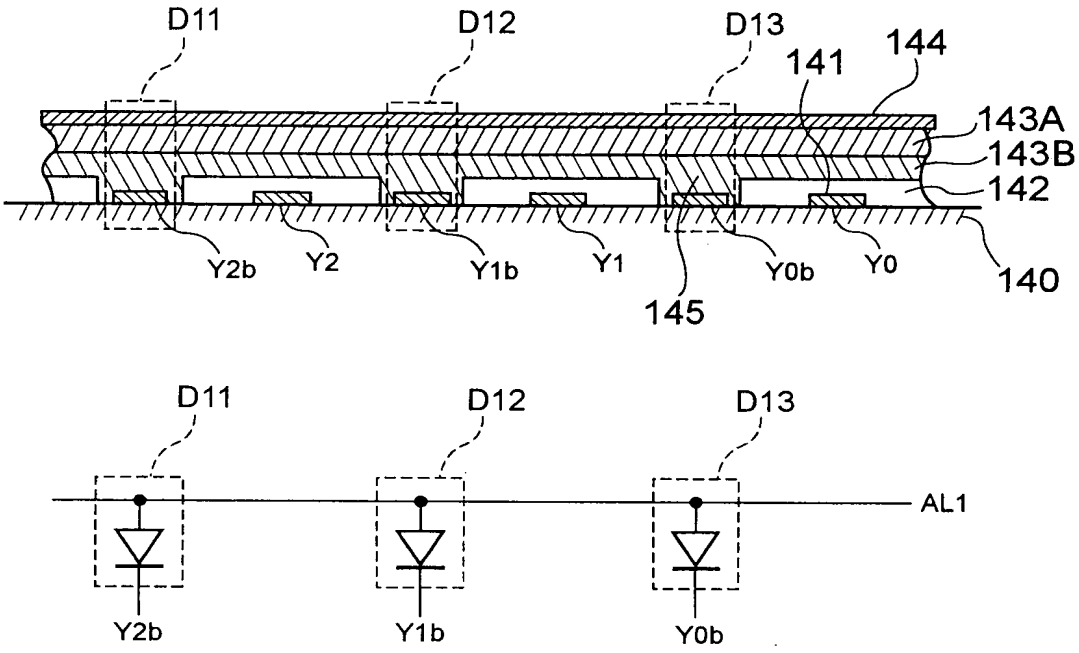

D11
D12
D13
144
141
143A
143B
142
Y2b
Y2
Y1b
Y1
Y0b
Y0
140
145
D11
D12
D13
AL1
Y2b
Y1b
Y0b

FIG. 20

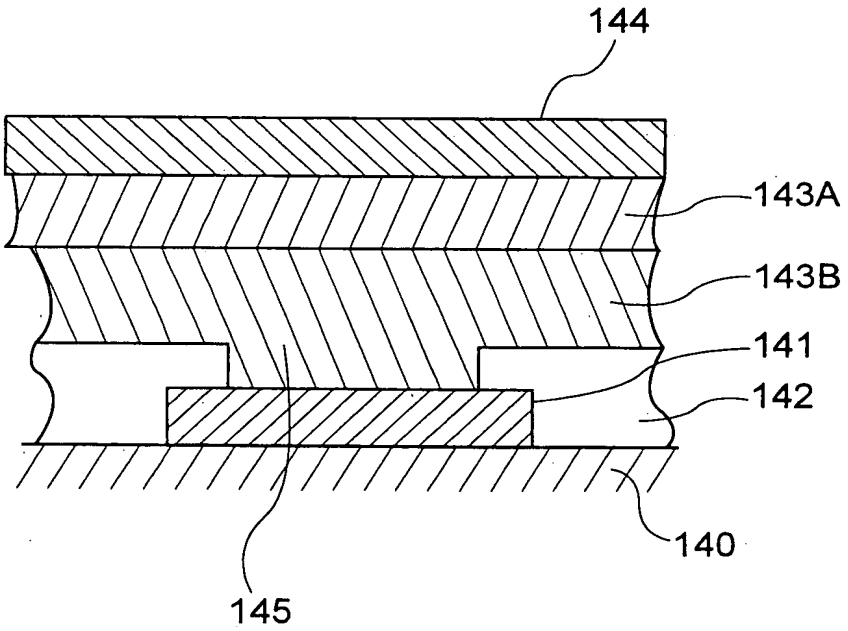

144
143A
143B
141
142
140
145

FIG. 21

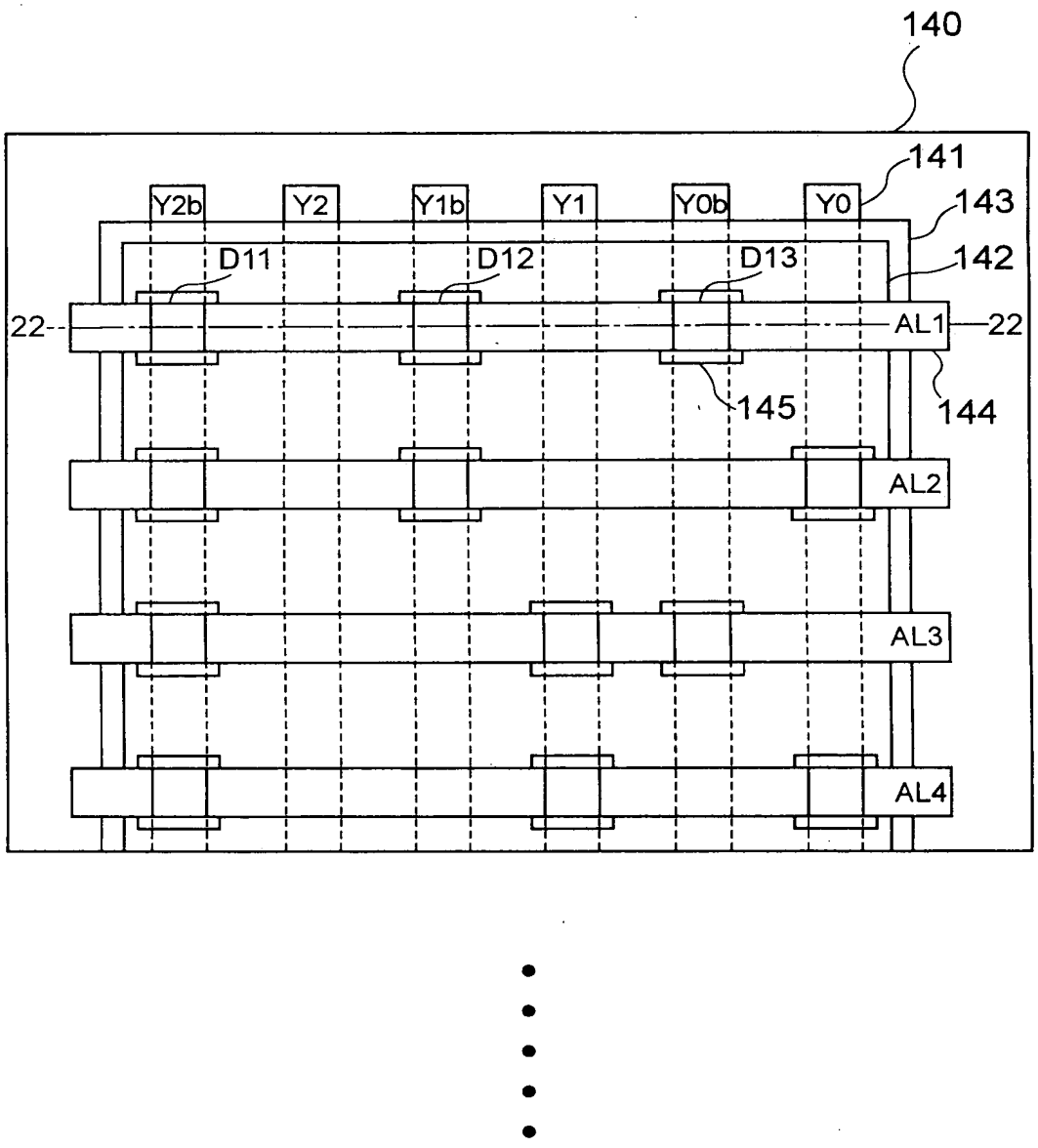

140
141
143
142
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
22
AL1
22
145
144
AL2
AL3
AL4

FIG. 22

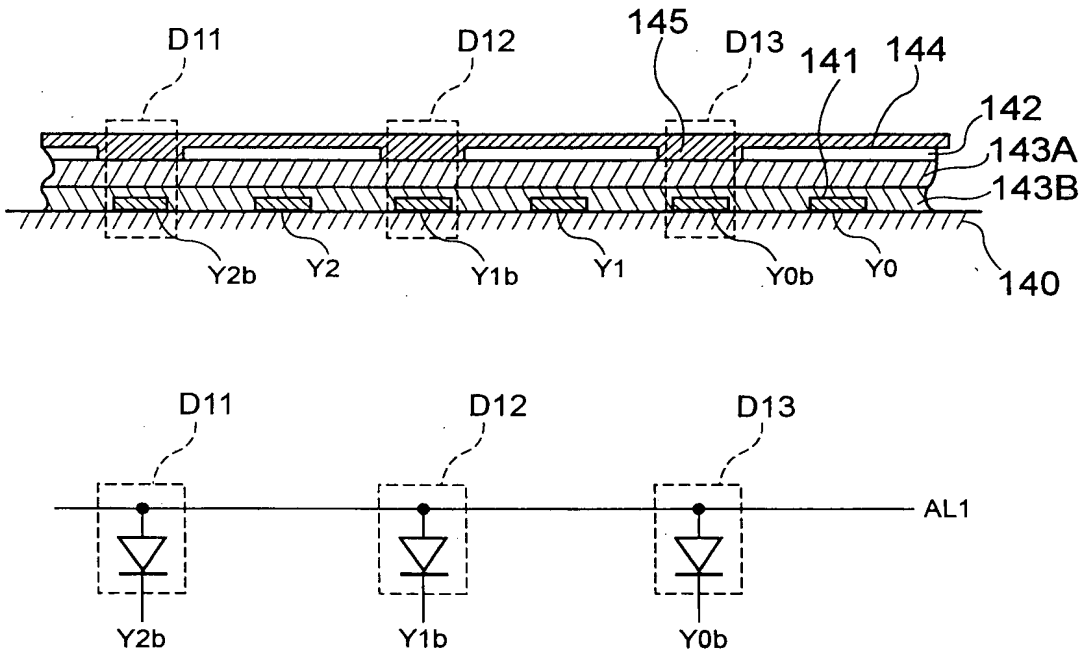

D11
D12
145
D13
141
144
142
143A
143B
Y2b
Y2
Y1b
Y1
Y0b
Y0
140
D11
D12
D13
AL1
Y2b
Y1b
Y0b

FIG. 23

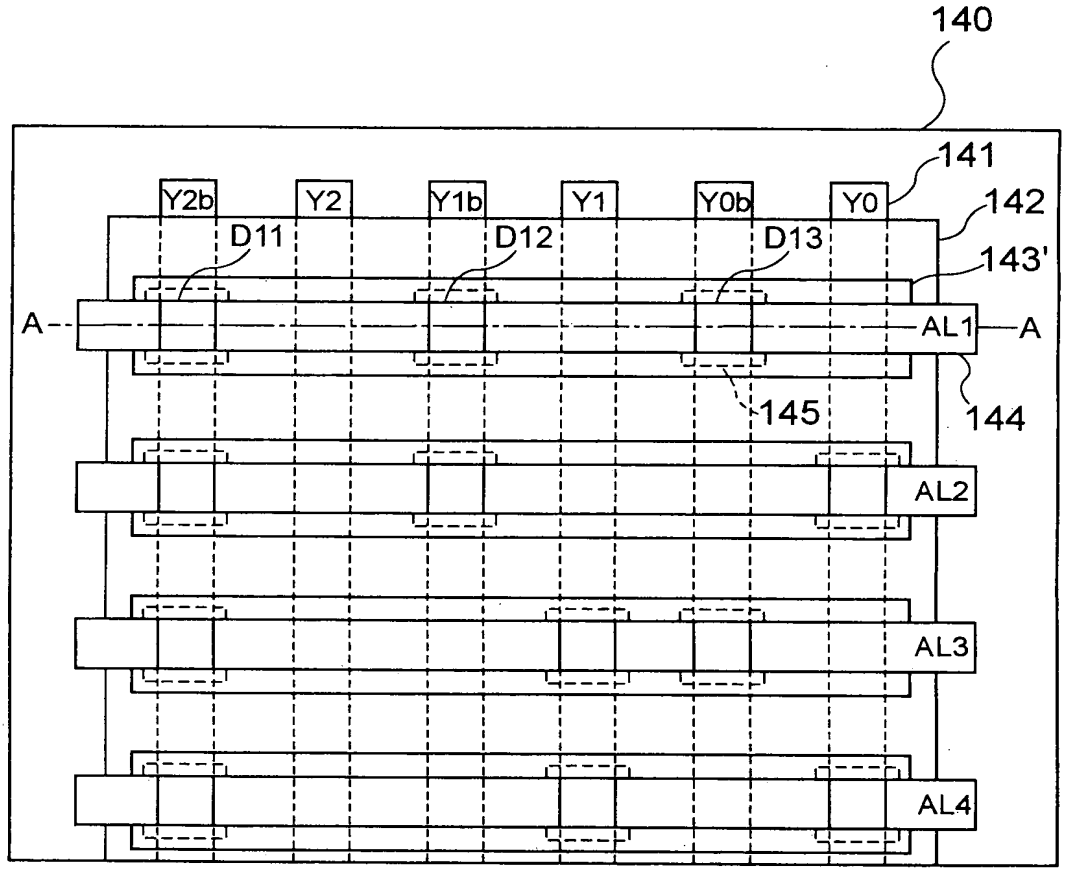

140
141
142
143'
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
A
AL1
A
145
144
AL2
AL3
AL4

FIG. 24

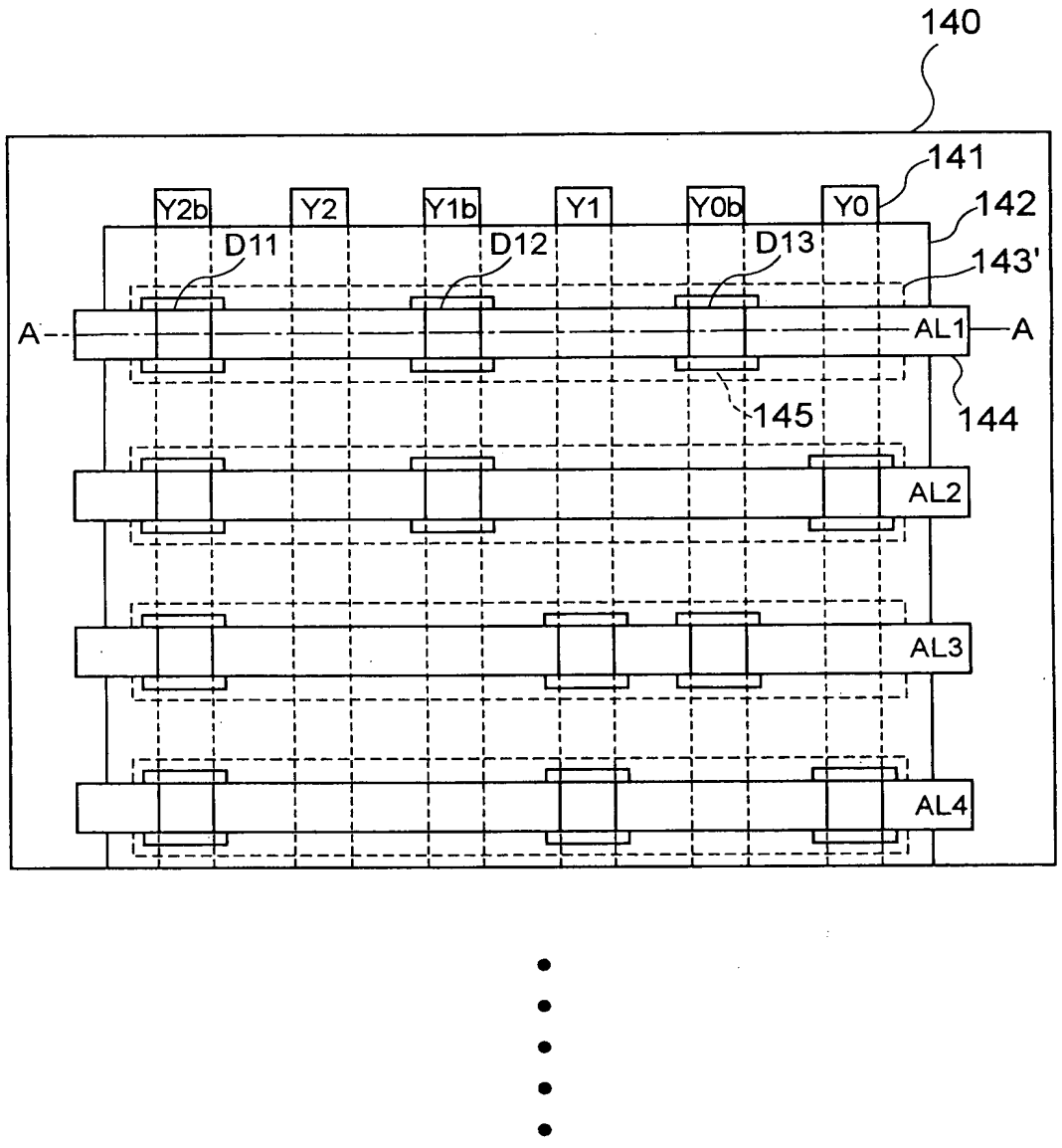

140
141
142
143'
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
A
AL1
A
145
144
AL2
AL3
AL4

FIG. 25

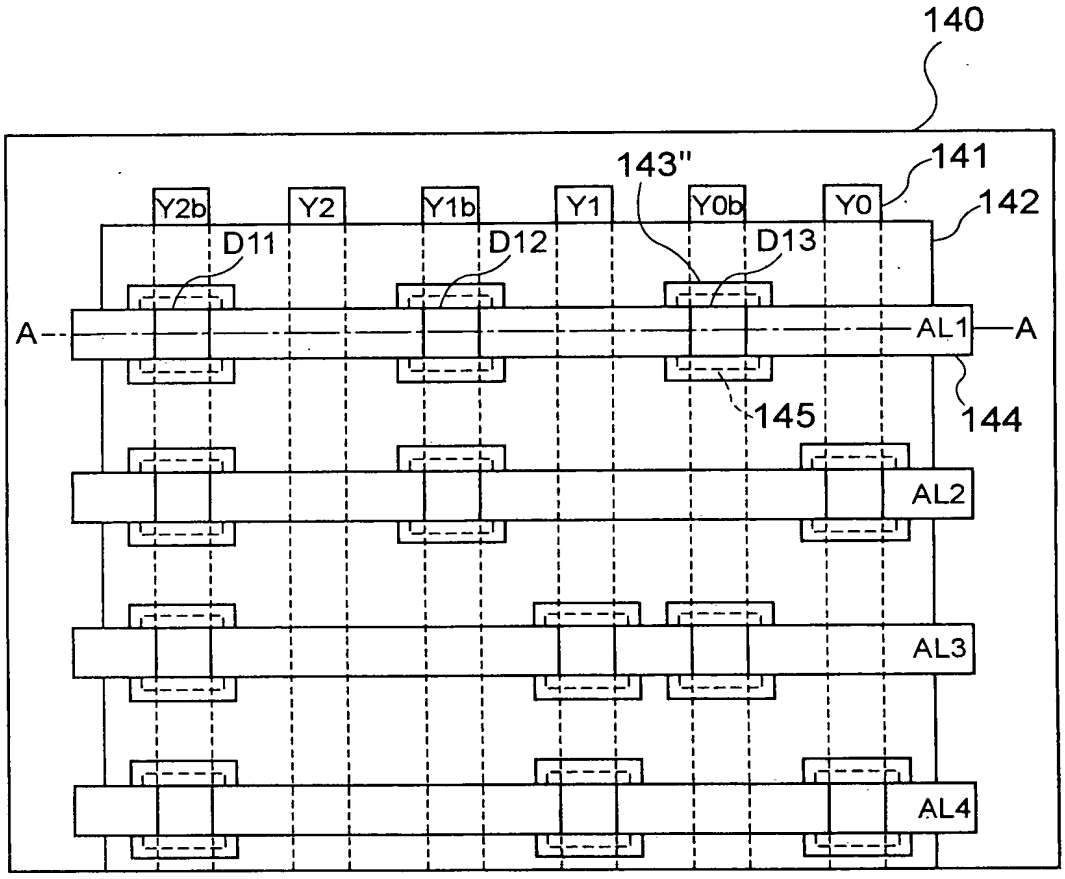

140
143"
141
142
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
A
AL1
A
145
144
AL2
AL3
AL4

FIG. 26

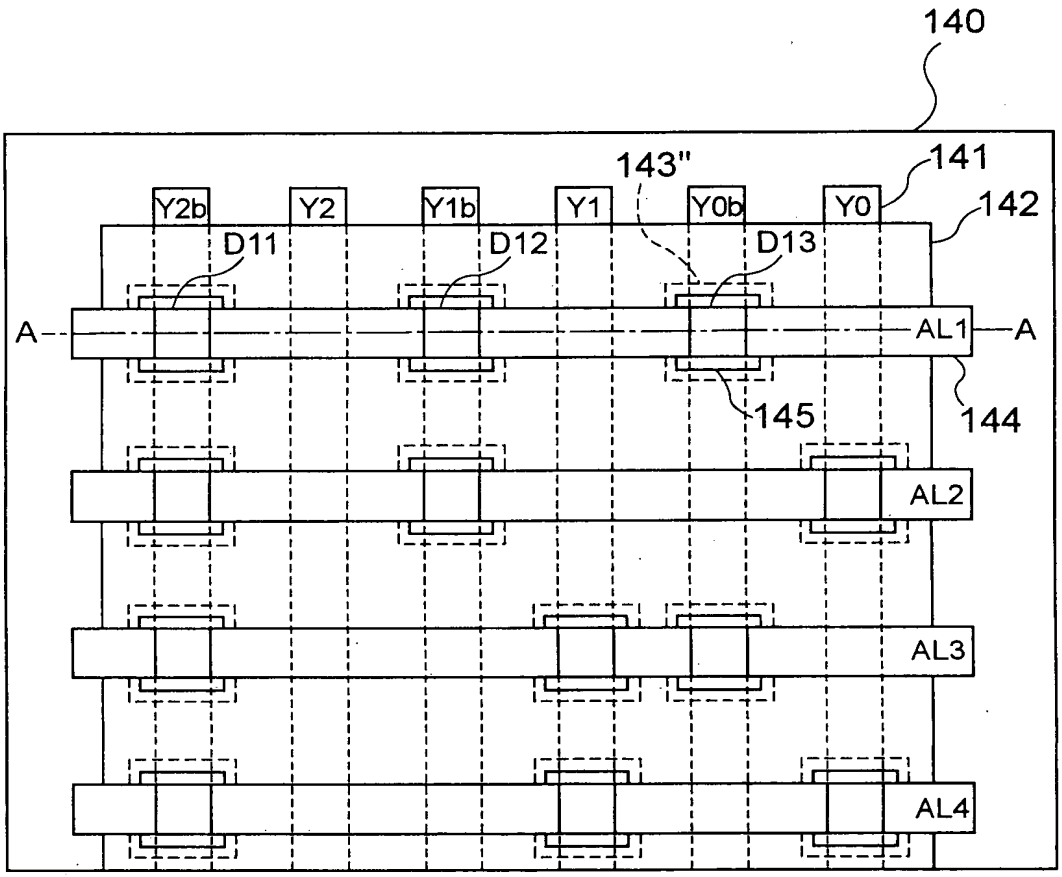

140
143"
141
142
Y2b
Y2
Y1b
Y1
Y0b
Y0
D11
D12
D13
A
AL1
A
145
144
AL2
AL3
AL4

FIG. 27

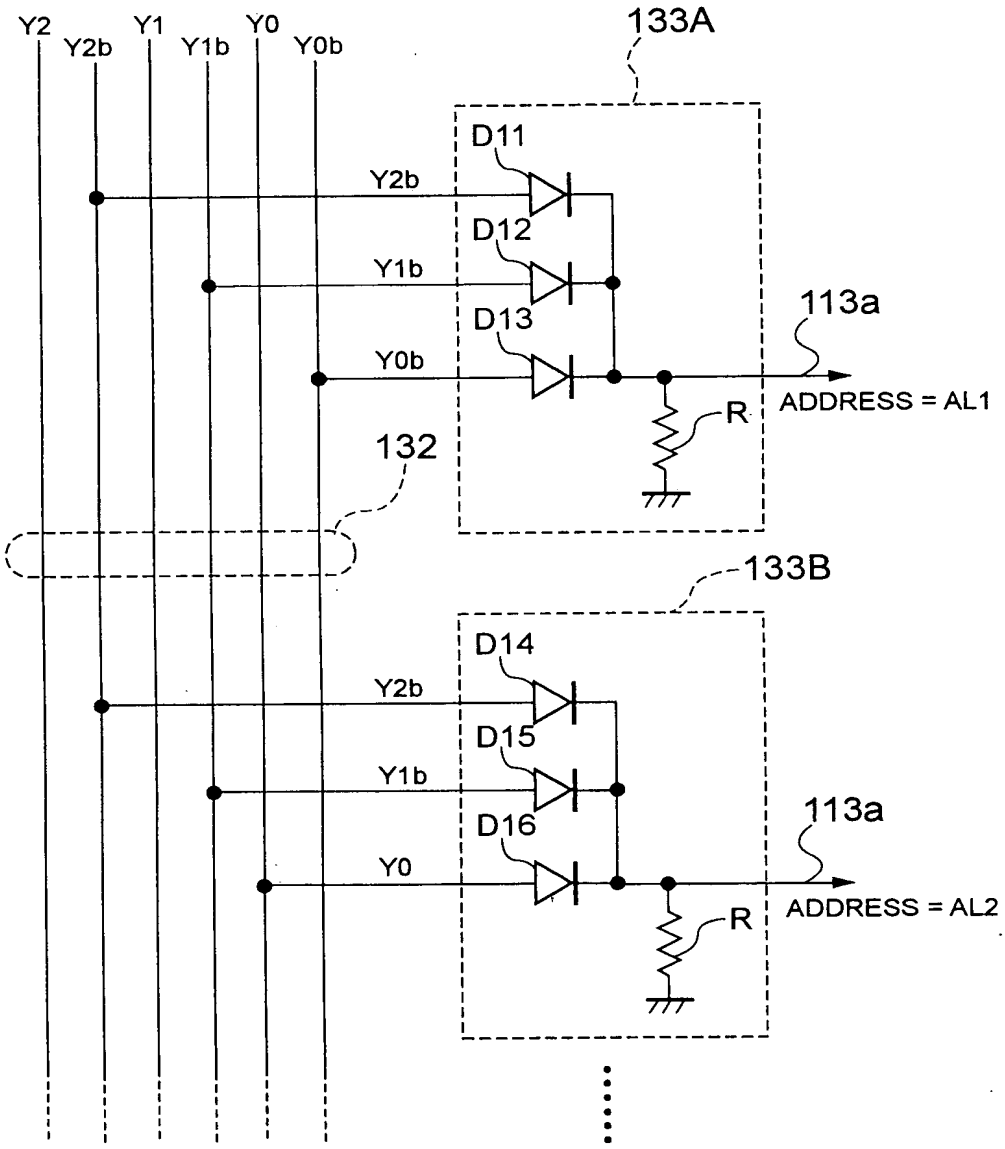

Y2
Y2b
Y1
Y1b
Y0
Y0b
133A
D11
Y2b
D12
Y1b
D13
Y0b
113a
ADDRESS = AL1
R
132
133B
D14
Y2b
D15
Y1b
D16
Y0
113a
ADDRESS = AL2
R

FIG. 28

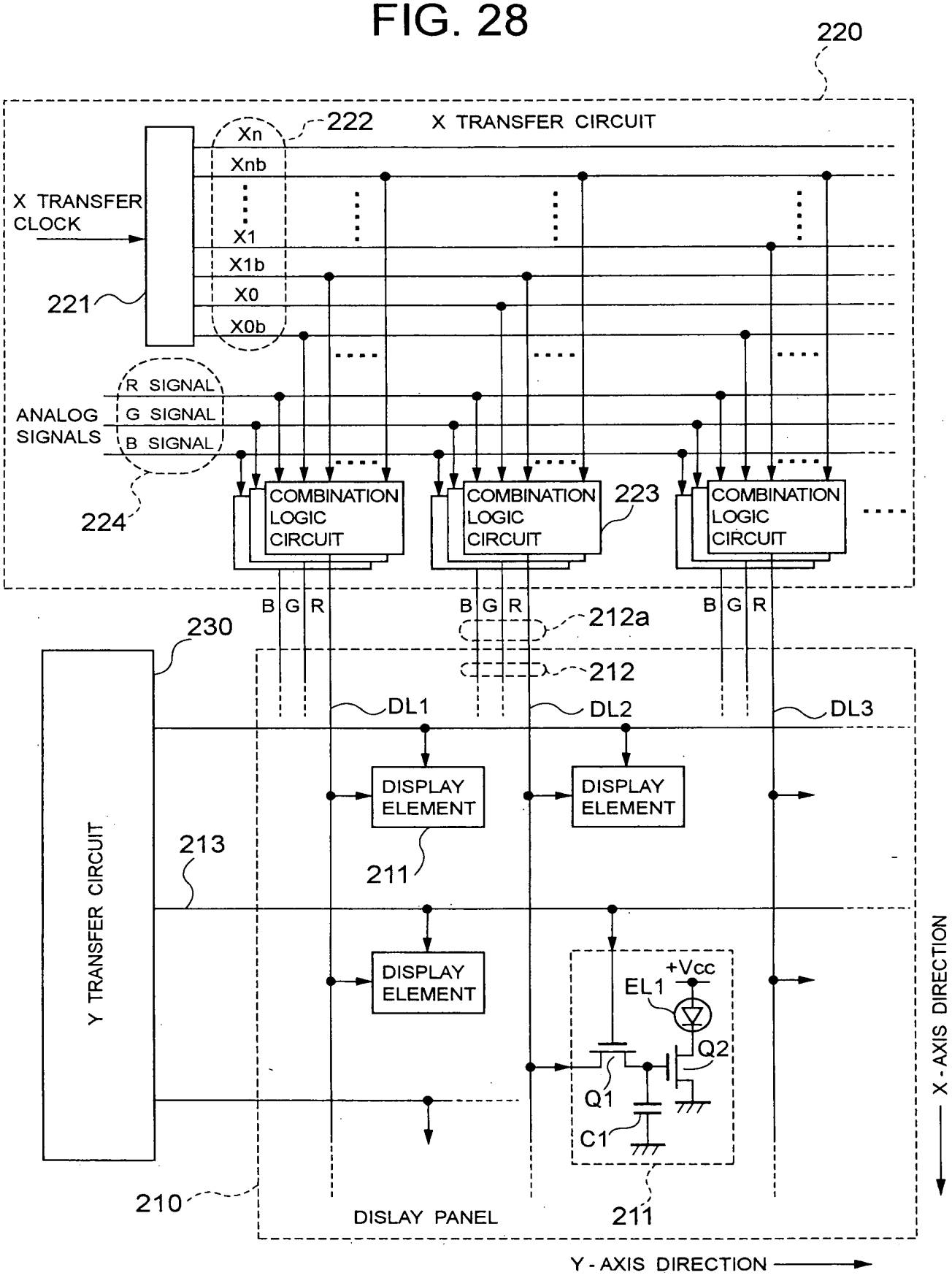

220
X TRANSFER CIRCUIT
222
Xn
Xnb
X1
X1b
X0
X0b
X TRANSFER CLOCK
221
R SIGNAL
G SIGNAL
B SIGNAL
ANALOG SIGNALS
224
COMBINATION LOGIC CIRCUIT
223
B G R
212a
212
230
DL1
DL2
DL3
DISPLAY ELEMENT
211
213
Y TRANSFER CIRCUIT
+Vcc
EL1
Q2
Q1
C1
210
DISLAY PANEL
X-AXIS DIRECTION
Y-AXIS DIRECTION

FIG. 29

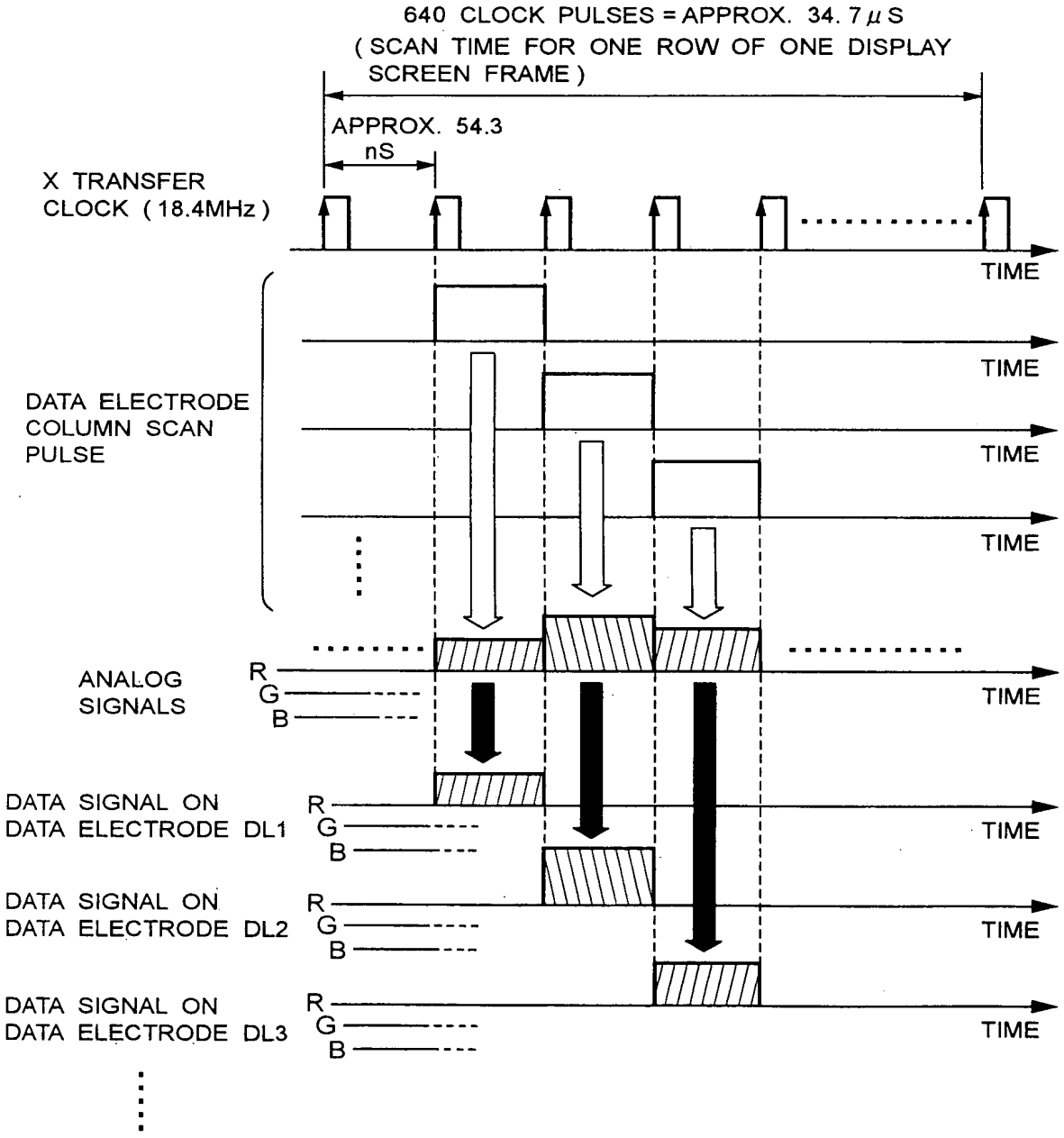

640 CLOCK PULSES = APPROX. 34.7 μS
(SCAN TIME FOR ONE ROW OF ONE DISPLAY SCREEN FRAME)
APPROX. 54.3 nS
X TRANSFER CLOCK (18.4MHz)
TIME
DATA ELECTRODE COLUMN SCAN PULSE
TIME
TIME
TIME
ANALOG SIGNALS
R
G
B
TIME
DATA SIGNAL ON DATA ELECTRODE DL1
R
G
B
TIME
DATA SIGNAL ON DATA ELECTRODE DL2
R
G
B
TIME
DATA SIGNAL ON DATA ELECTRODE DL3
R
G
B
TIME

FIG. 30

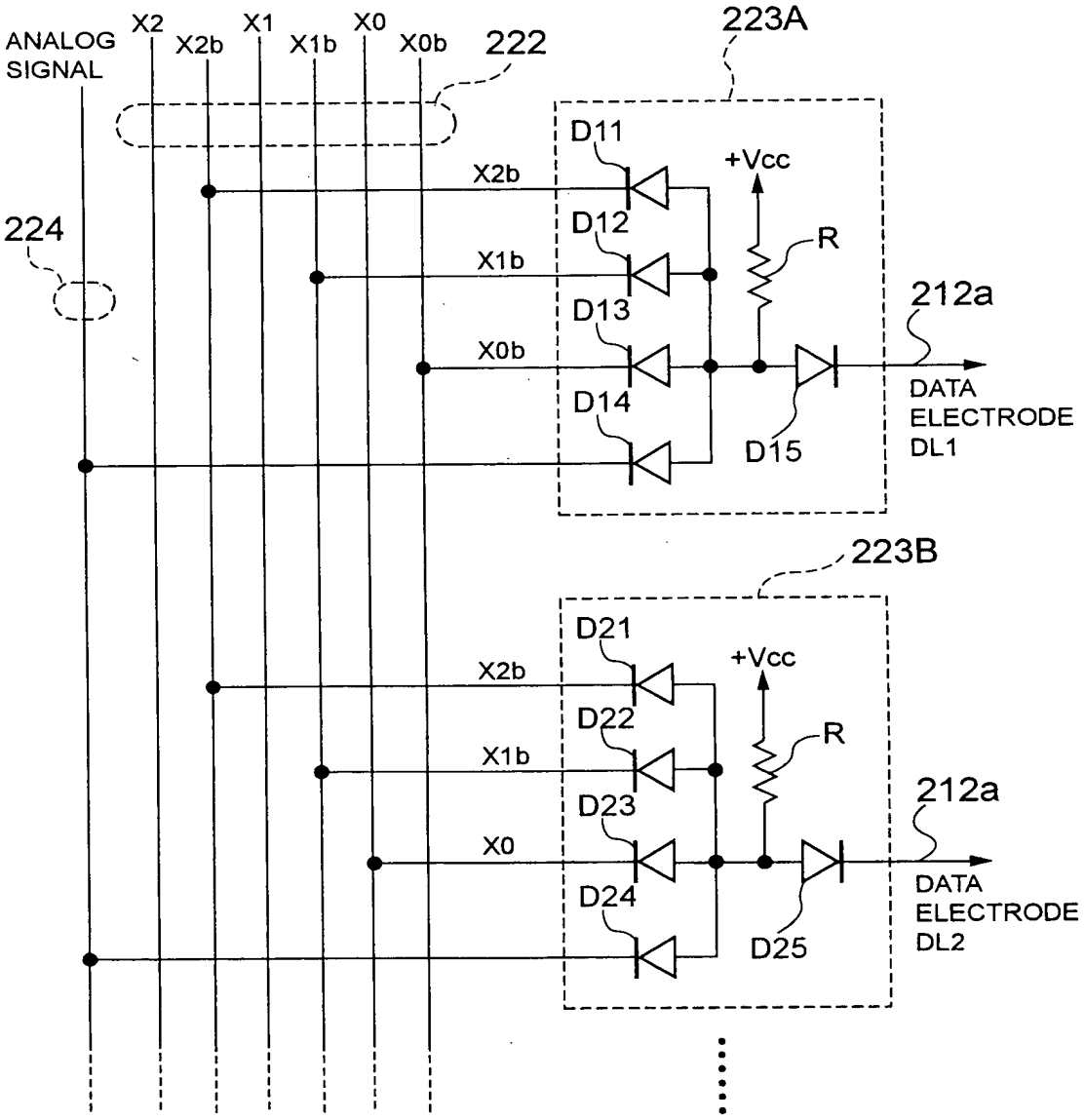

ANALOG
SIGNAL
X2
X2b
X1
X1b
X0
X0b
222
223A
224
D11
+Vcc
X2b
D12
R
X1b
212a
D13
X0b
D14
DATA
ELECTRODE
DL1
D15
223B
D21
+Vcc
X2b
D22
R
X1b
212a
D23
X0
D24
DATA
ELECTRODE
DL2
D25

FIG. 31

DATA ELECTRODE ADDRESS (DL)	RELATION BETWEEN CODE GROUP SUPERPOSED ON ADDRESS LINE GROUP (X2 TO X0 AND X2b TO X0b) AND DECODED ADDRESS					
	BINARY CODE			INVERTED BINARY CODE		
	X2	X1	X0	X2b	X1b	X0b
DL=1	0	0	0	1	1	1
DL=2	0	0	1	1	1	0
DL=3	0	1	0	1	0	1
DL=4	0	1	1	1	0	0
DL=5	1	0	0	0	1	1
DL=6	1	0	1	0	1	0
DL=7	1	1	0	0	0	1
DL=8	1	1	1	0	0	0

FIG. 32

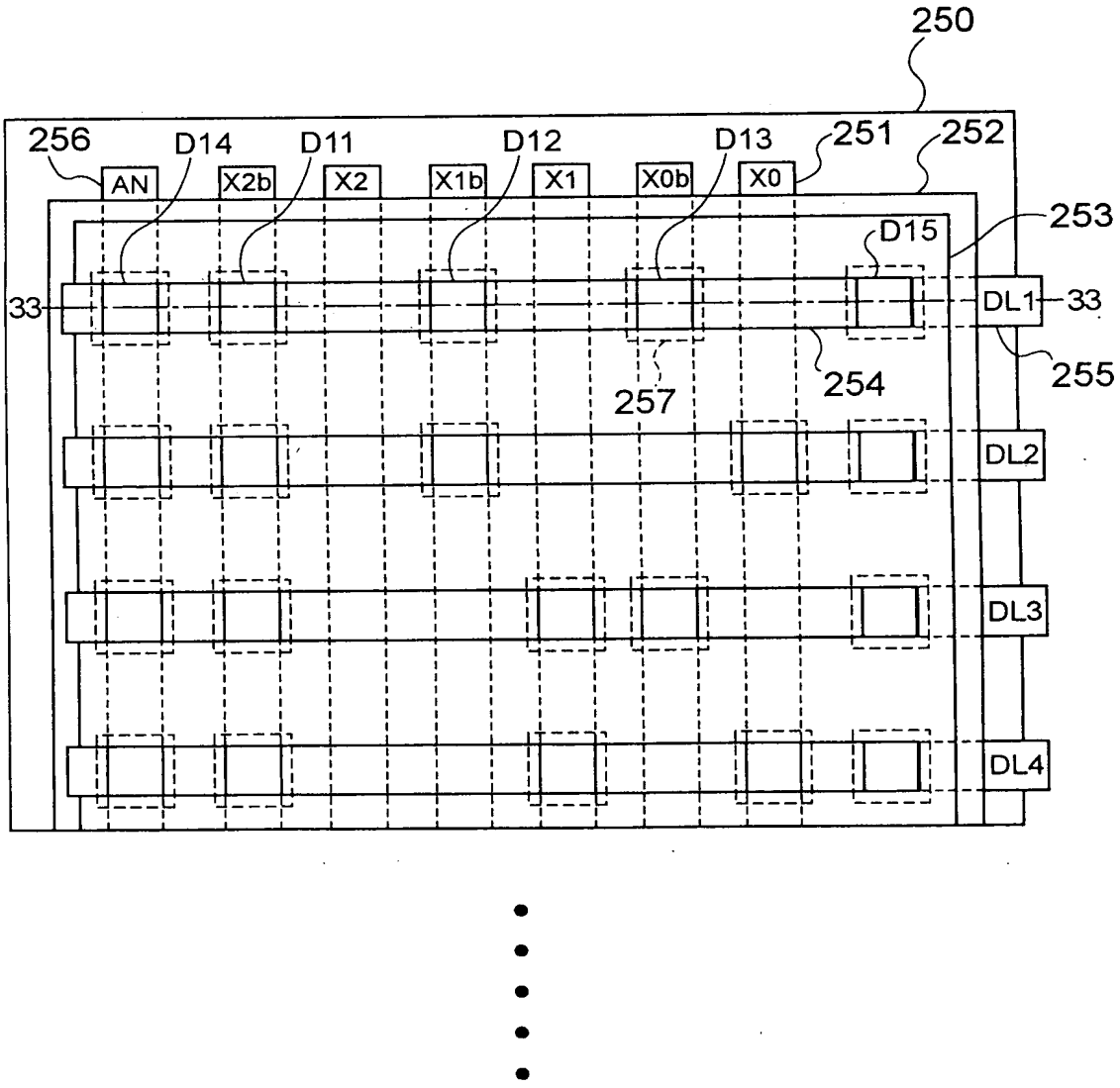

250
256
D14
D11
D12
D13
251
252
AN
X2b
X2
X1b
X1
X0b
X0
253
D15
33
DL1
33
255
257
254
DL2
DL3
DL4

FIG. 33

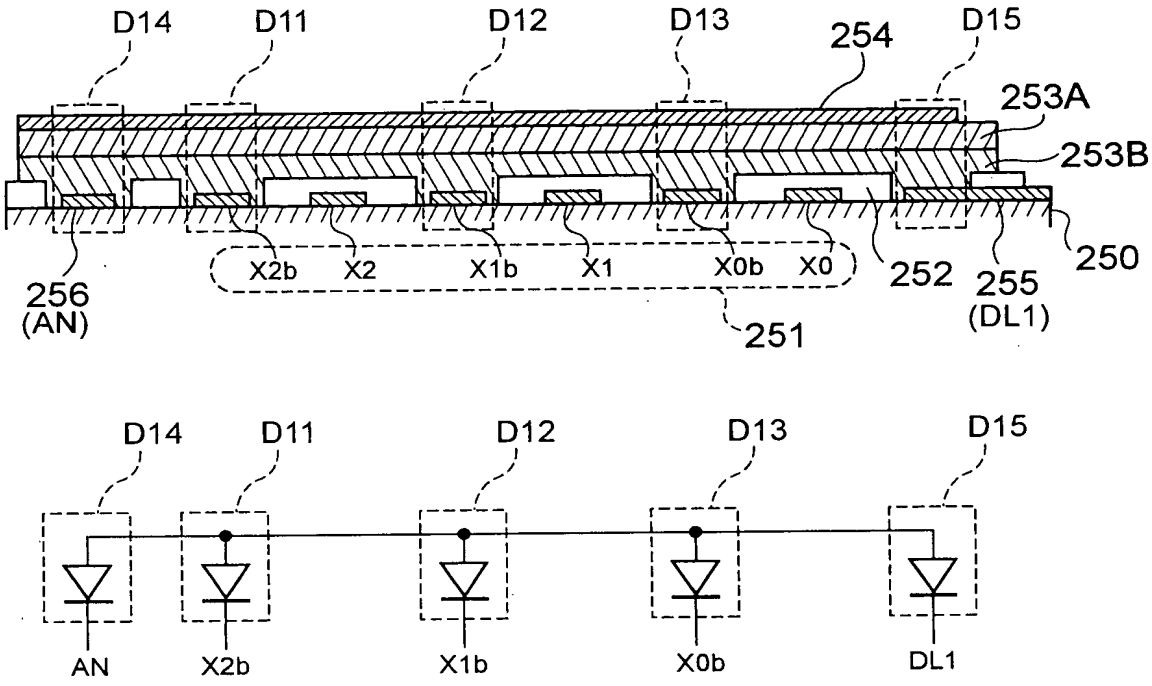

D14
D11
D12
D13
254
D15
253A
253B
250
256
(AN)
X2b
X2
X1b
X1
X0b
X0
252
255
(DL1)
251
D14
D11
D12
D13
D15
AN
X2b
X1b
X0b
DL1

FIG. 34

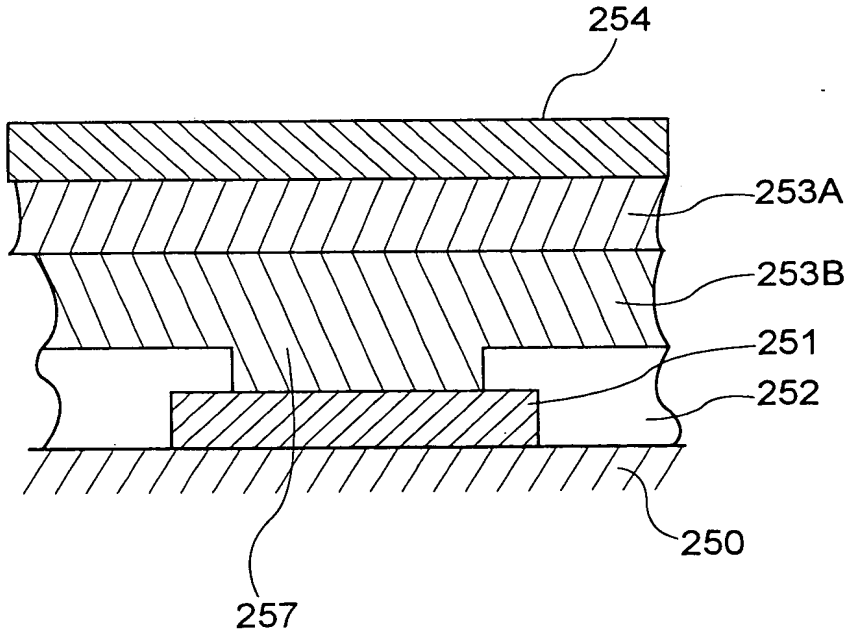

254
253A
253B
251
252
250
257

FIG. 35

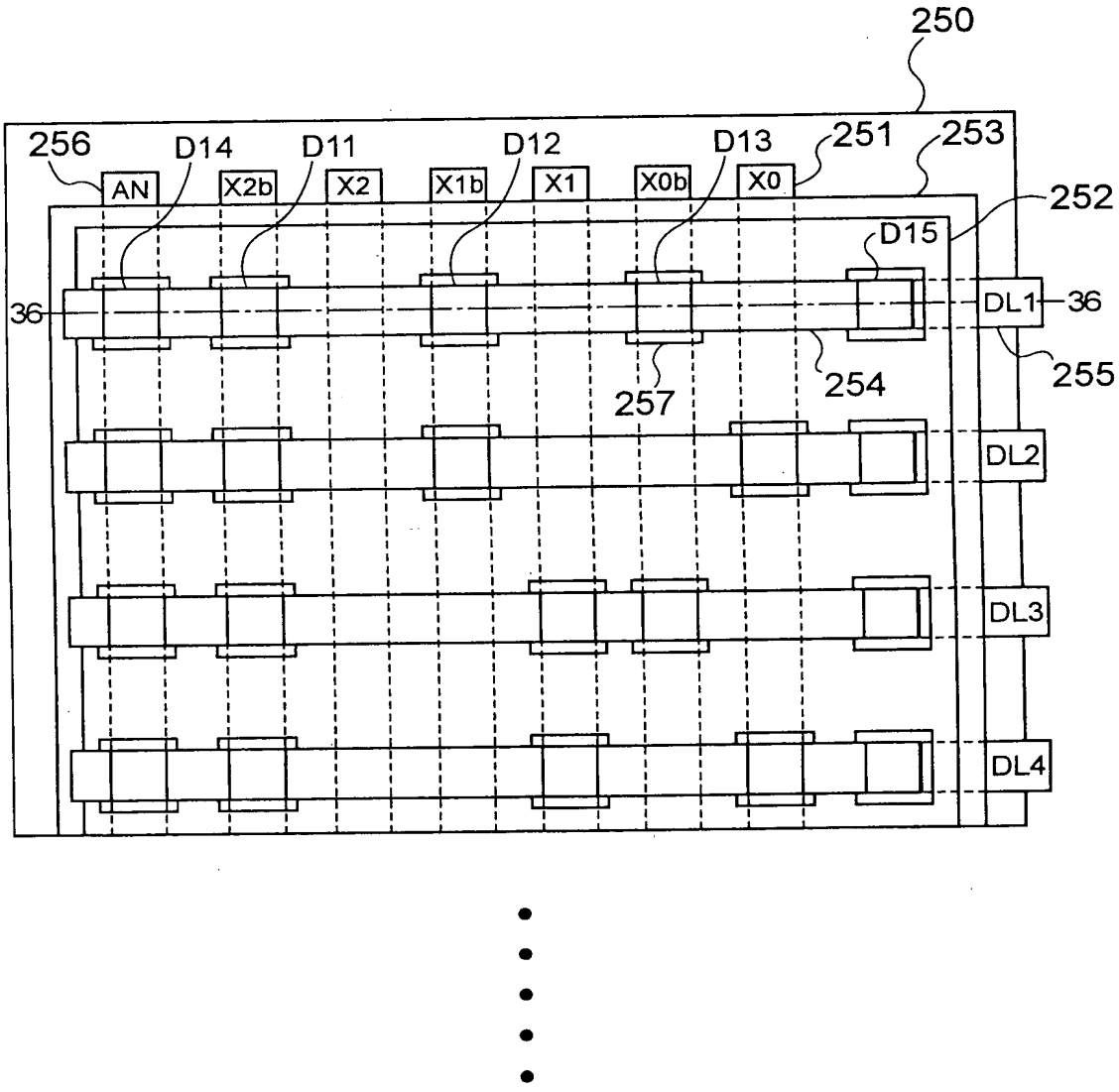
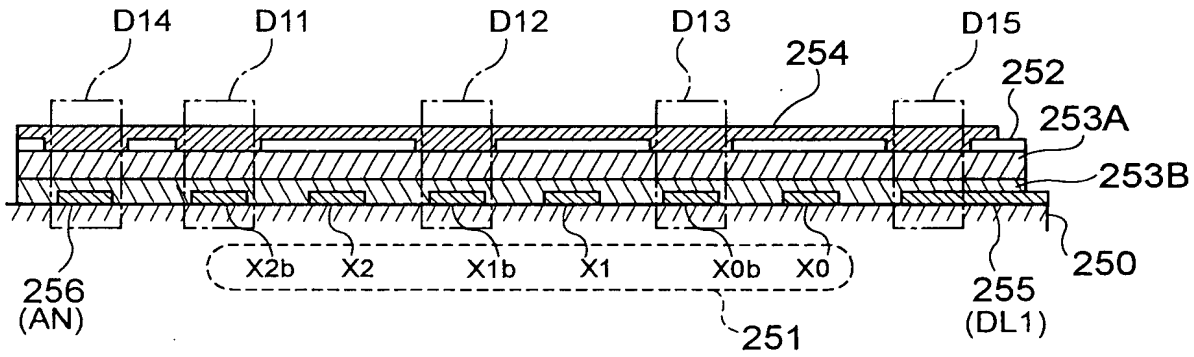

250
256
D14
D11
D12
D13
251
253
AN
X2b
X2
X1b
X1
X0b
X0
252
D15
36
DL1
36
255
257
254
DL2
DL3
DL4

FIG. 36


D14
D11
D12
D13
D15
254
252
253A
253B
250
256
(AN)
X2b
X2
X1b
X1
X0b
X0
251
255
(DL1)

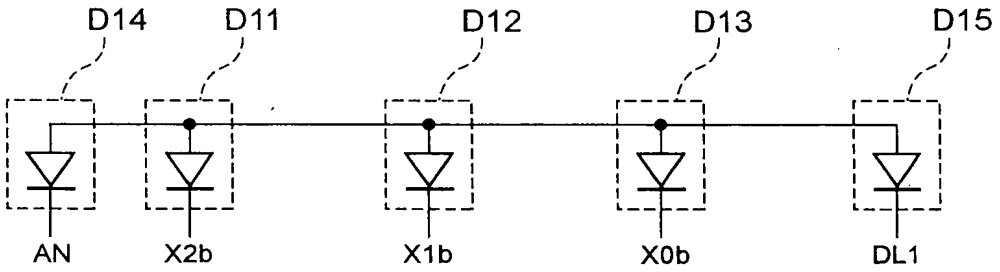

D14
D11
D12
D13
D15
AN
X2b
X1b
X0b
DL1

FIG. 37

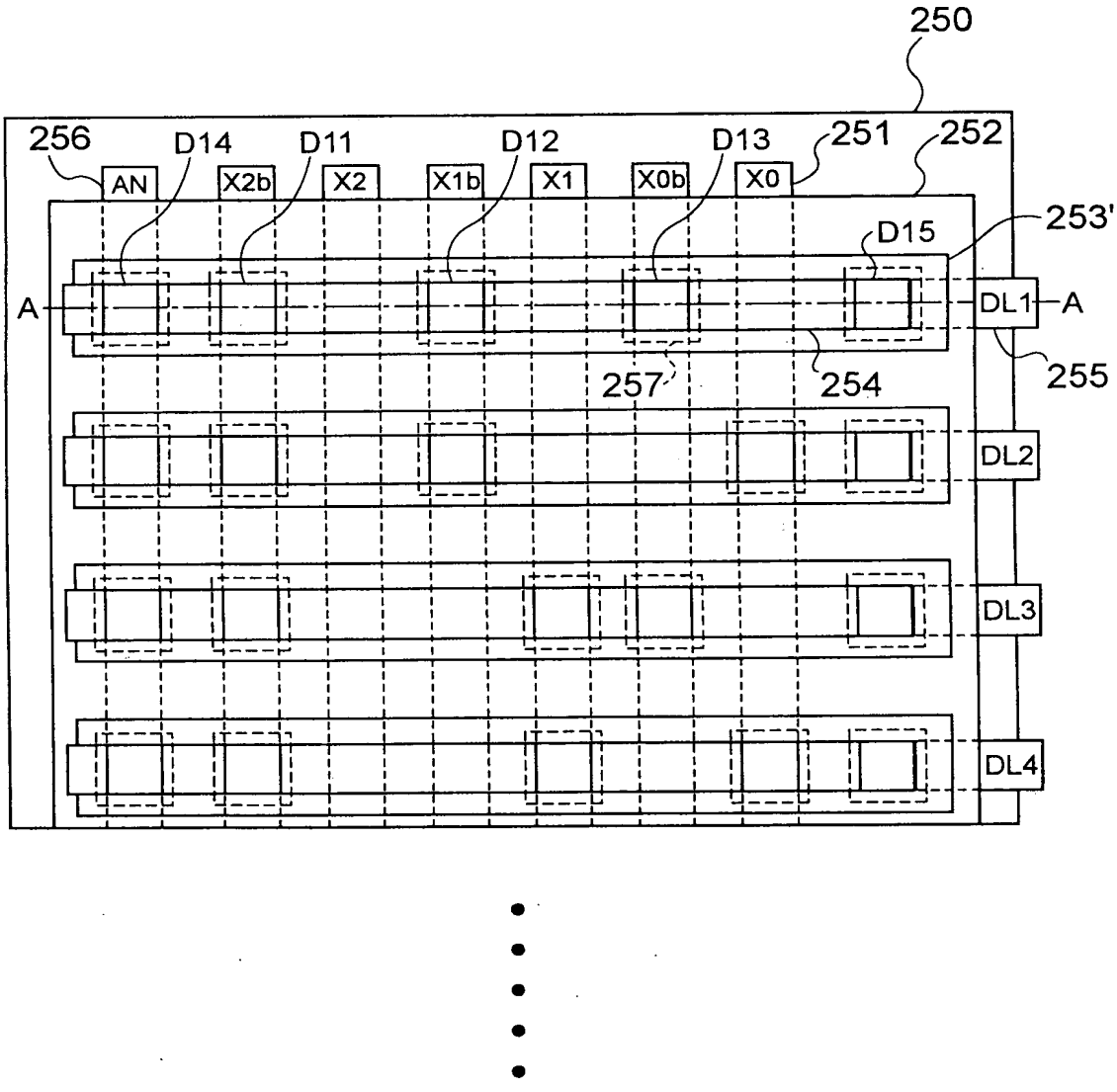

250
256
D14
D11
D12
D13
251
252
AN
X2b
X2
X1b
X1
X0b
X0
D15
253'
A
DL1
A
257
254
255
DL2
DL3
DL4

FIG. 38

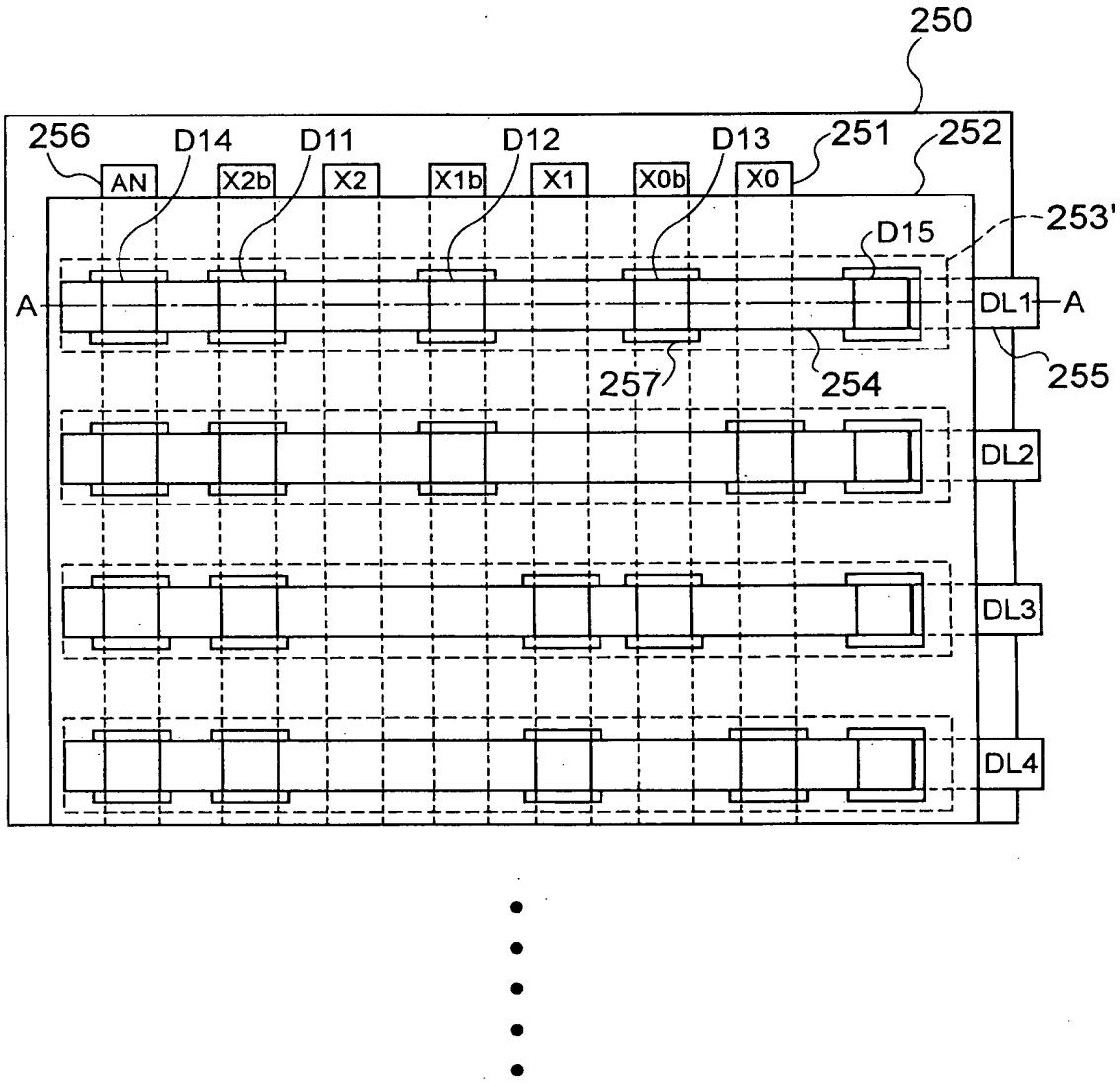

250
256
D14
D11
D12
D13
251
252
AN
X2b
X2
X1b
X1
X0b
X0
D15
253'
A
DL1
A
255
257
254
DL2
DL3
DL4

FIG. 39

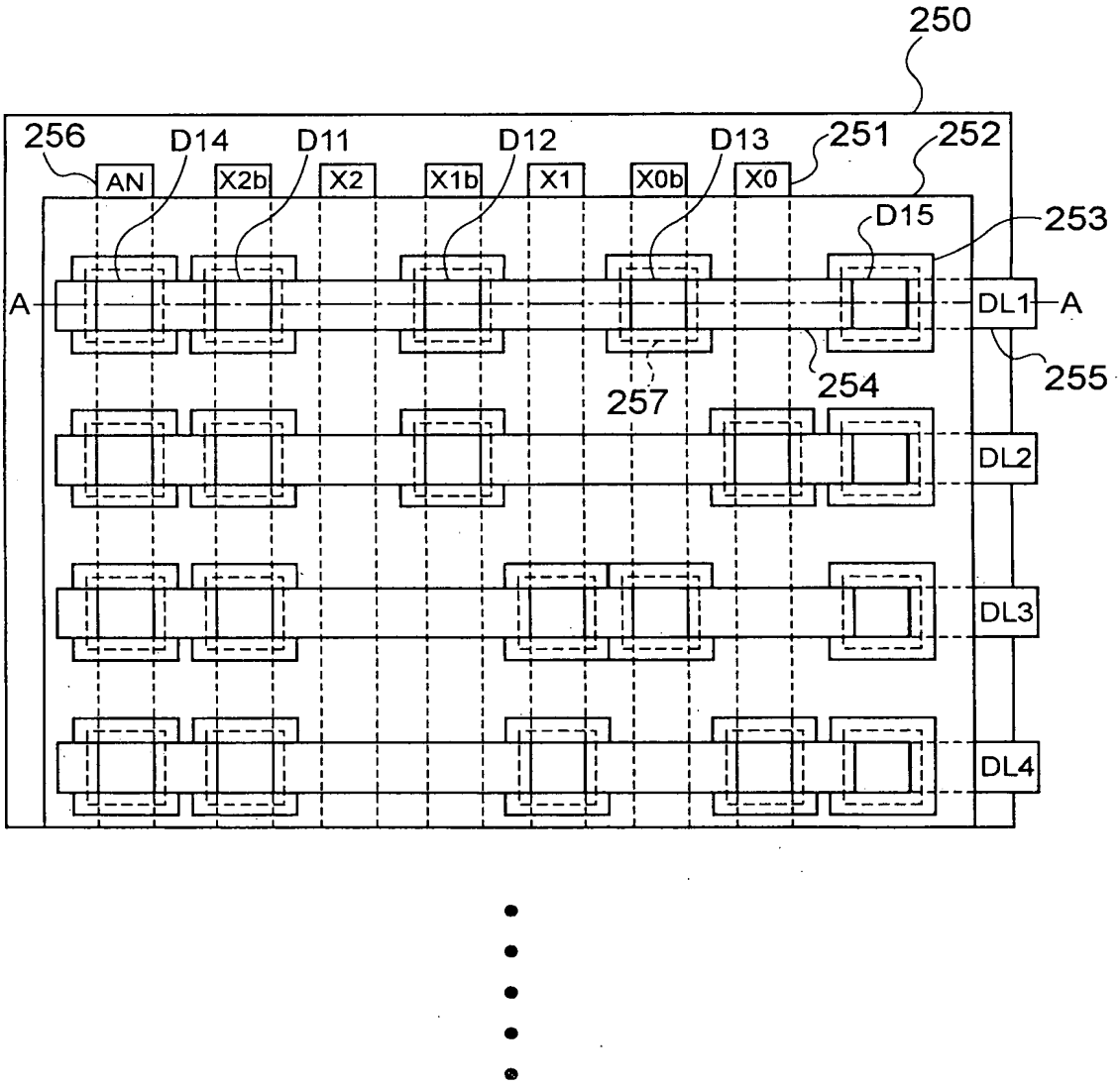

250
256
D14
D11
D12
D13
251
252
AN
X2b
X2
X1b
X1
X0b
X0
D15
253
A
DL1
A
255
257
254
DL2
DL3
DL4

FIG. 40

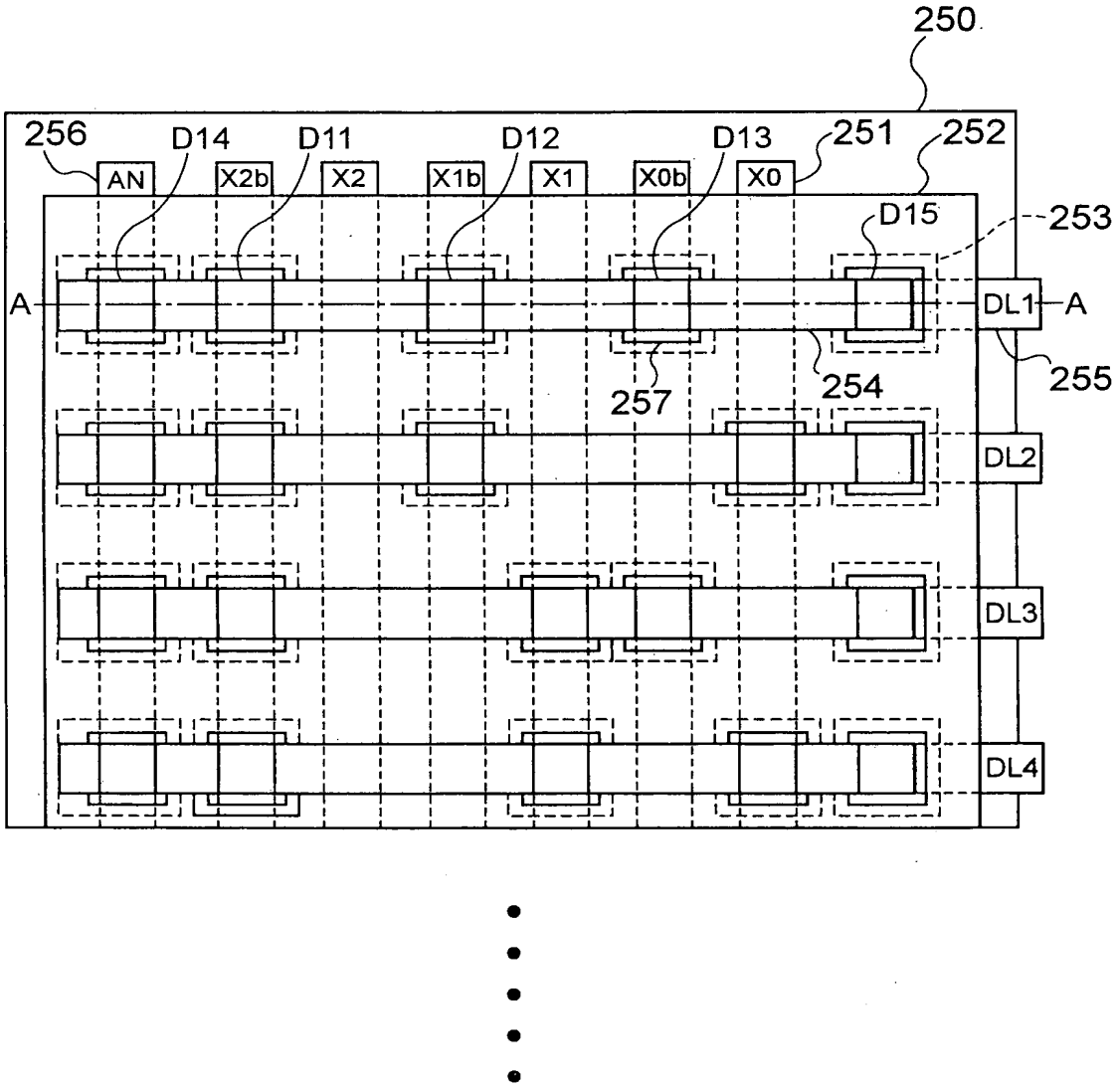
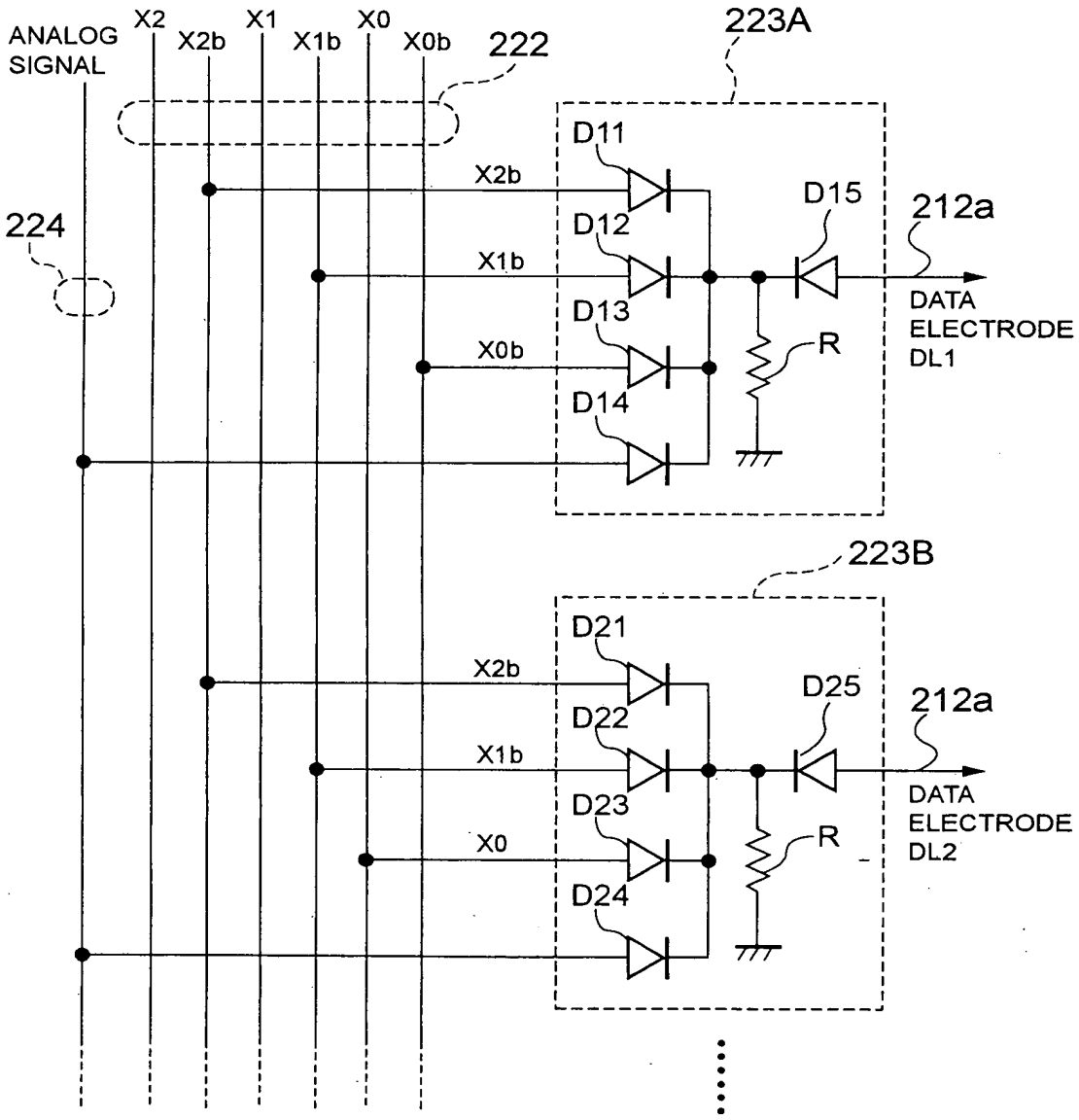

250
256
D14
D11
D12
D13
251
252
AN
X2b
X2
X1b
X1
X0b
X0
D15
253
A
DL1
A
255
257
254
DL2
DL3
DL4

FIG. 41


ANALOG
SIGNAL
X2
X2b
X1
X1b
X0
X0b
222
223A
224
D11
D12
D13
D14
D15
X2b
X1b
X0b
212a
DATA
ELECTRODE
DL1
R
223B
D21
D22
D23
D24
D25
X2b
X1b
X0
212a
DATA
ELECTRODE
DL2
R